

Compal Confidential

QAL30 Project

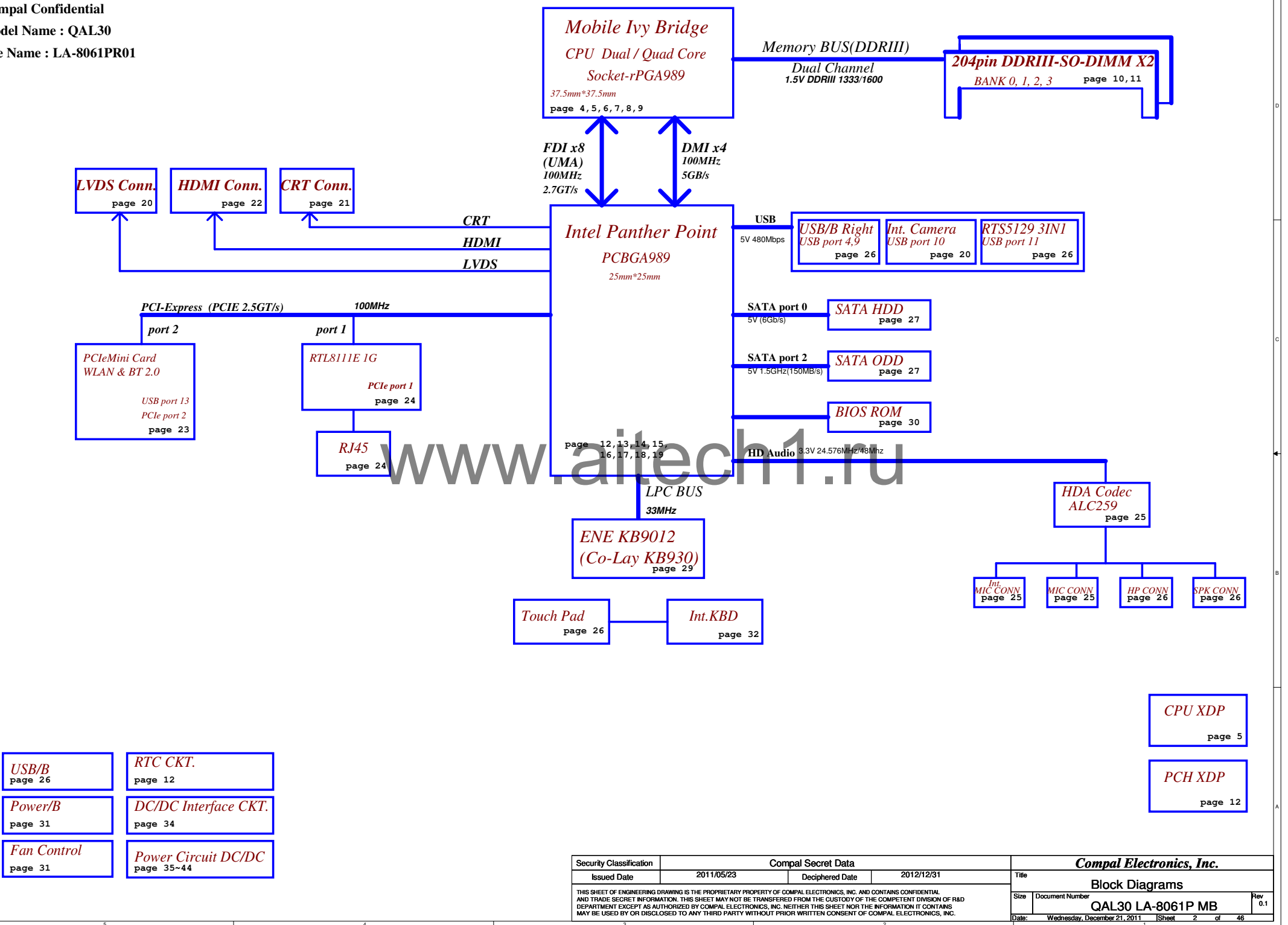
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LA-8061P REV 0.4 Schematic

Intel Ivy Bridge/Panther Point

2012-01-13 Rev. 0.4

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Issued Date	2011/05/23	Deciphered Date	2012/12/31	Title	Cover Sheet
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Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.168V	0.250 V	0.362 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	QAL30
1	
2	
3	
4	
5	
6	
7	

SMBUS Control Table

	SOURCE	MINI1	BATT 0001 011x b	SODIMM 1001 000x b	SODIMM 1001 010x b	PCH		
EC_SMB_CK1 EC_SMB_DA1	KB930 KB9012	X	V	X	X	X		
EC_SMB_CK2 EC_SMB_DA2	KB930 KB9012	X	X	X	X	V		
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	V	V			
PCH_SML1CLK PCH_SML1DATA	PCH	X	X	X	X			

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	TPM
PCI3	None
PCI4	None

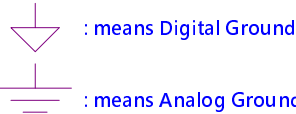
PCH

USB PORT#	DESTINATION
0	USB2/3 (Left Hand disc front)
1	USB2/3 (Left Hand disc back)
2	None
3	None
4	USB2 (Right Hand side front)
5	None
6	None
7	None
8	None
9	USB2 (Left Hand side back)
10	CAMERA
11	Card Reader
12	None
13	BT Comb

OPTIMUS: XDP@/D@

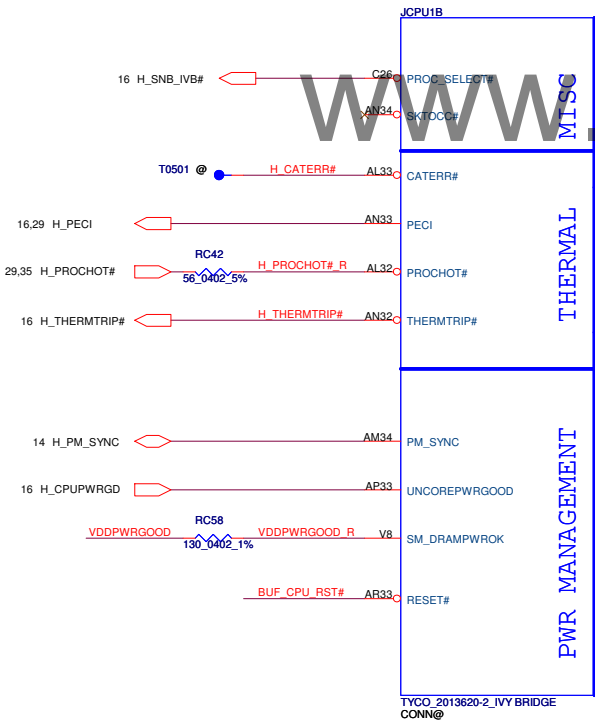
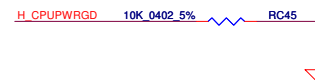
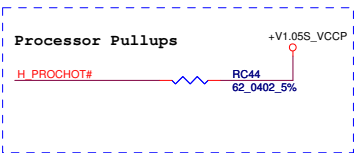
CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_A	VGA		
	CLKOUT_PEG_B	None		

Symbol Note :

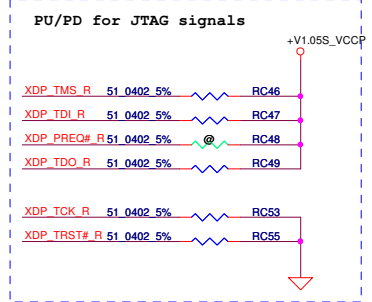
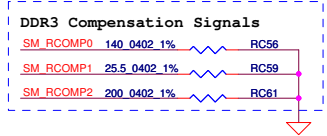
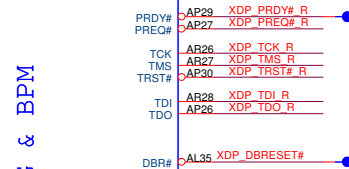
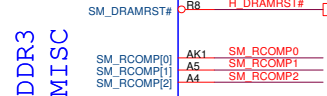
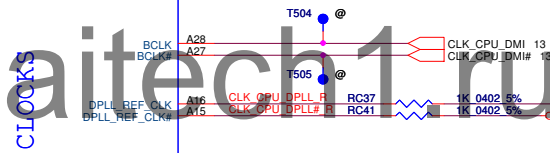
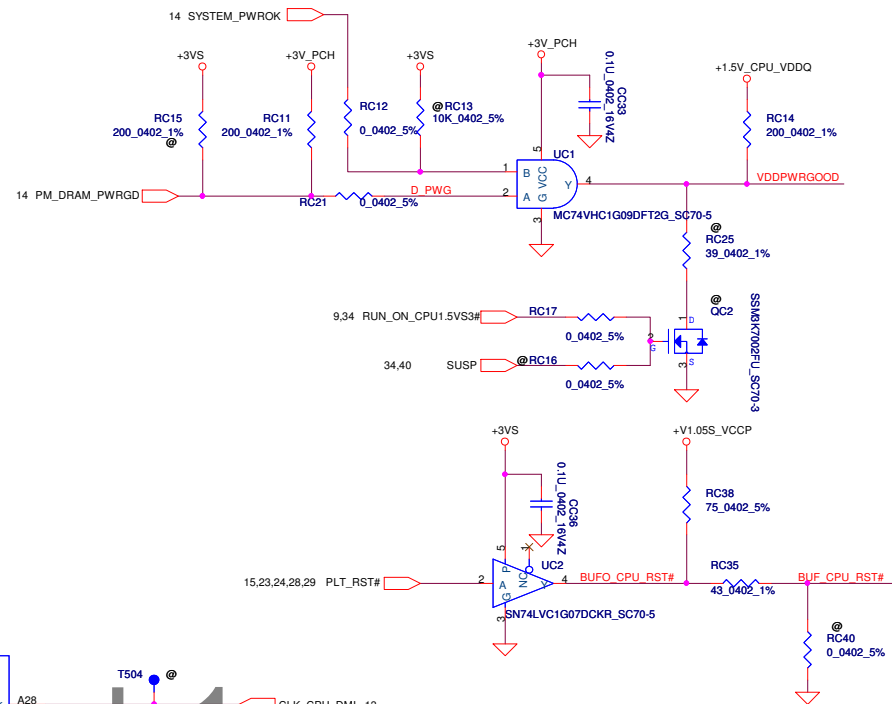


SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	LAN
Lane 2	WLAN
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

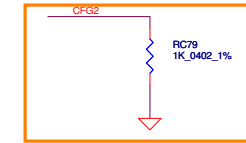
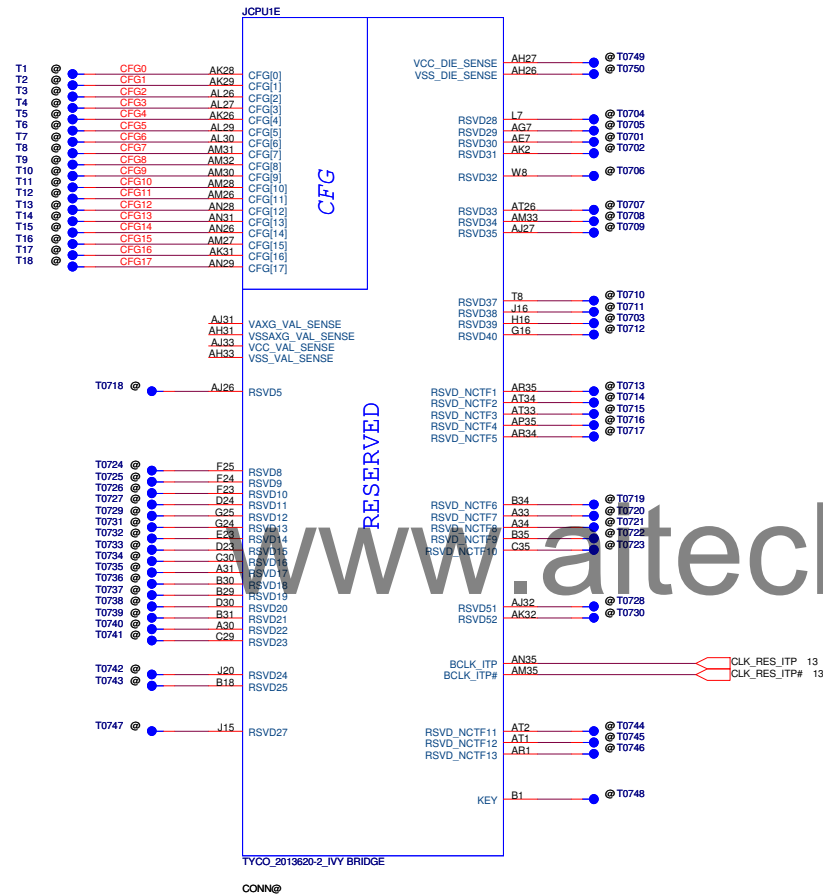


TYCO_2013620-2_IVV BRIDGE
CONN@

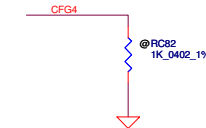


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				PROCESSOR(2/6) PM,XDP,CLK	
				Size	Document Number
				Custom	QAL30 LA-8061P MB
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				Rev	0.1

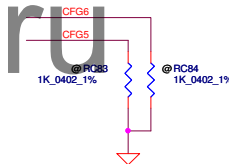
CFG Straps for Processor



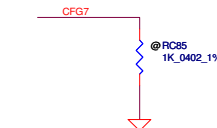
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

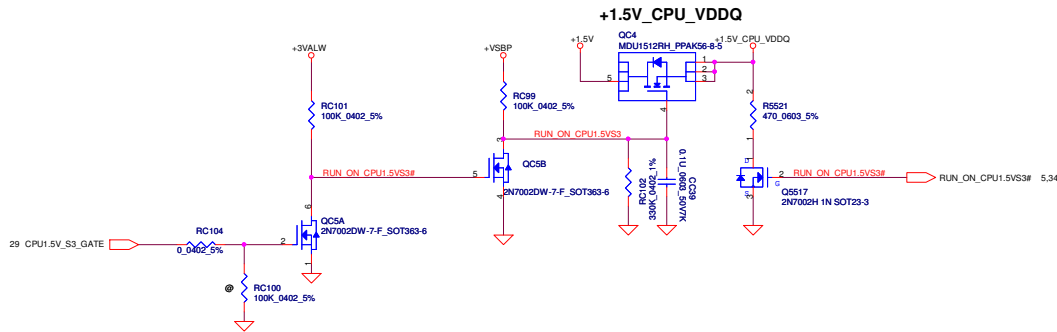


PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

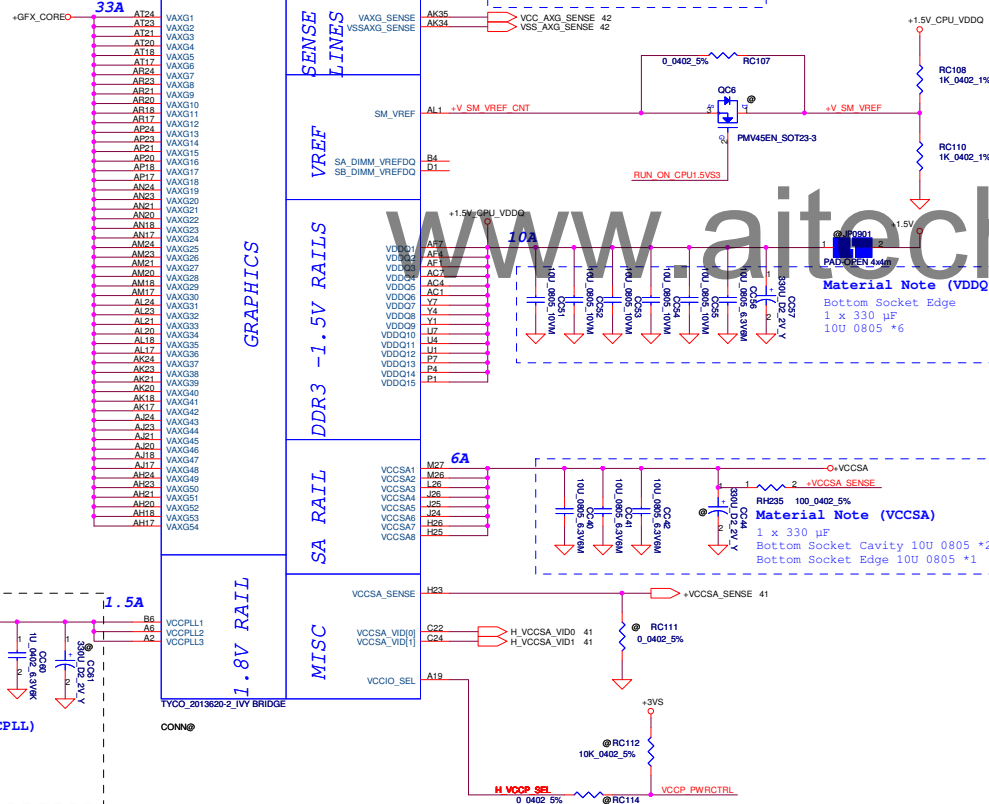


PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following RESETB de assertion 0: PEG Wait for BIOS for training

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				PROCESSOR(4/6) RSVD,CFG	
				Size	
Custom		Document Number		Rev	
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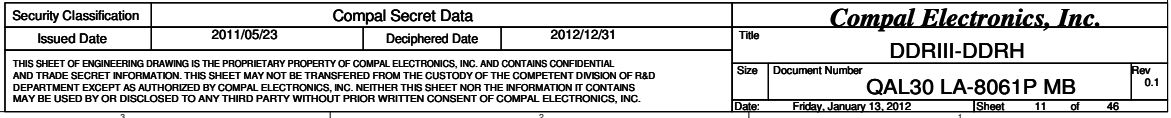
POWER

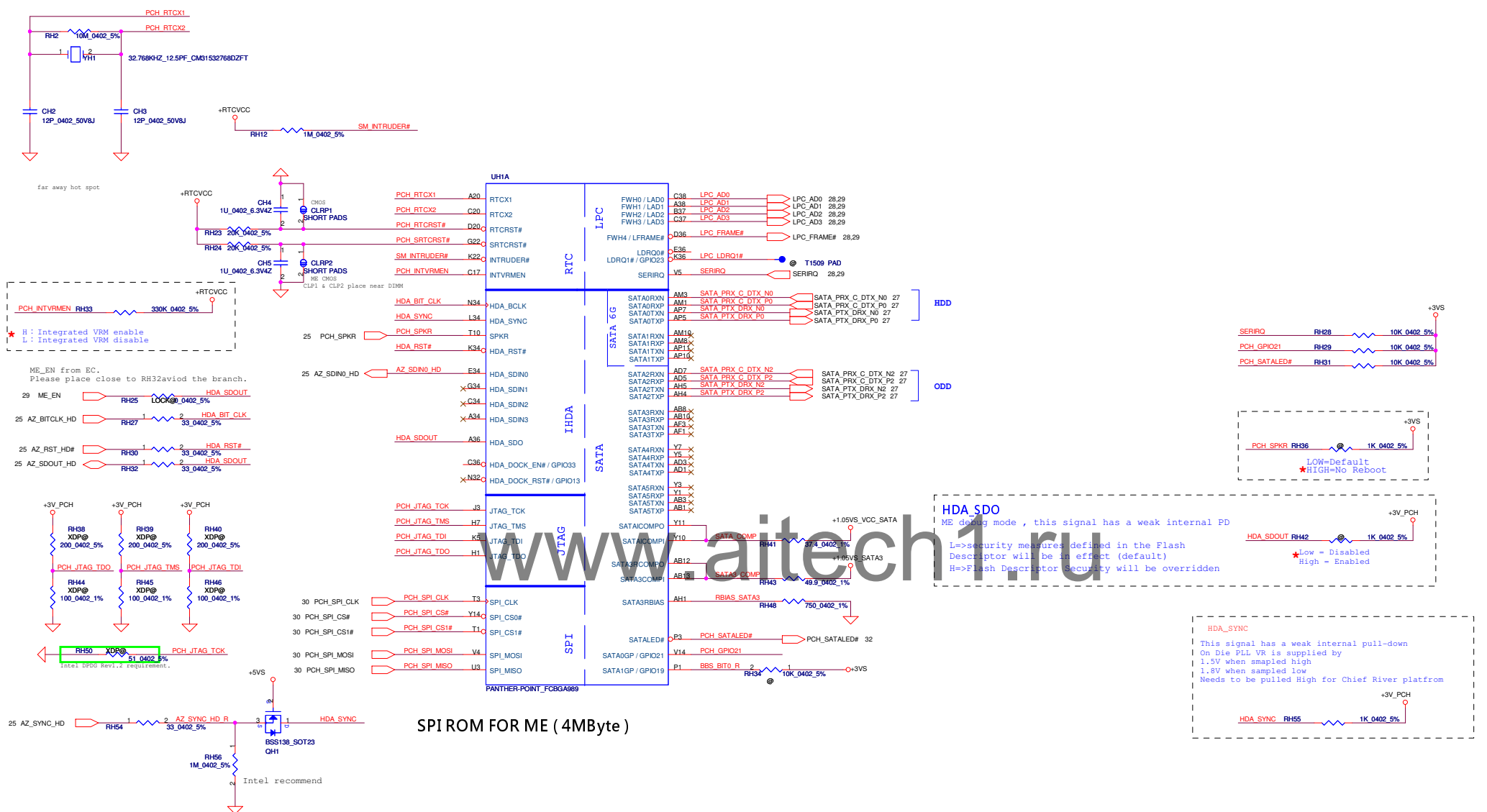


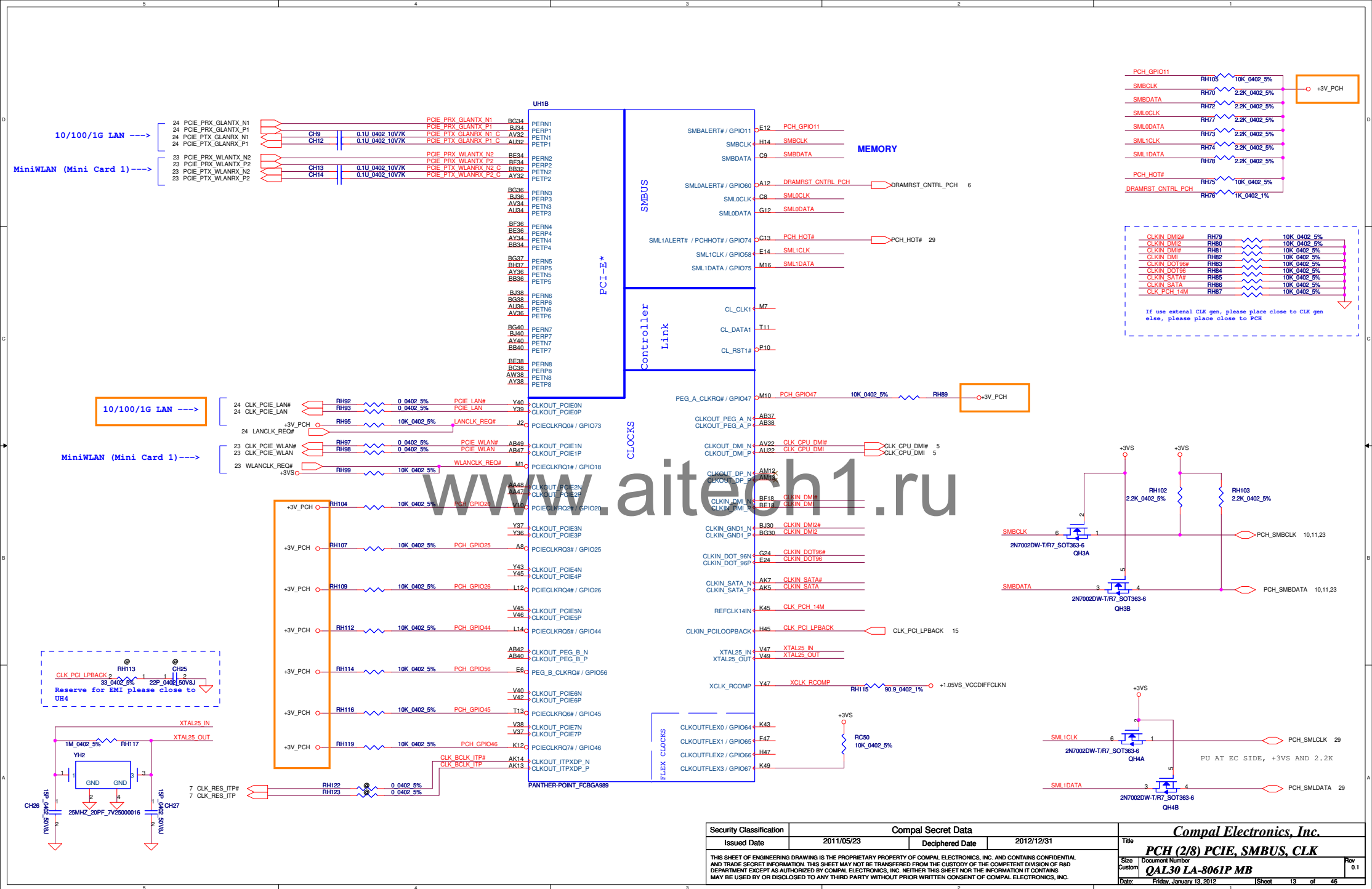
IVY Bridge drives VCCIO_SEL low
 VCCP_PWRCTRL:0

Sandy Bridge is NC for A19
 VCCP_PWRCTRL:1

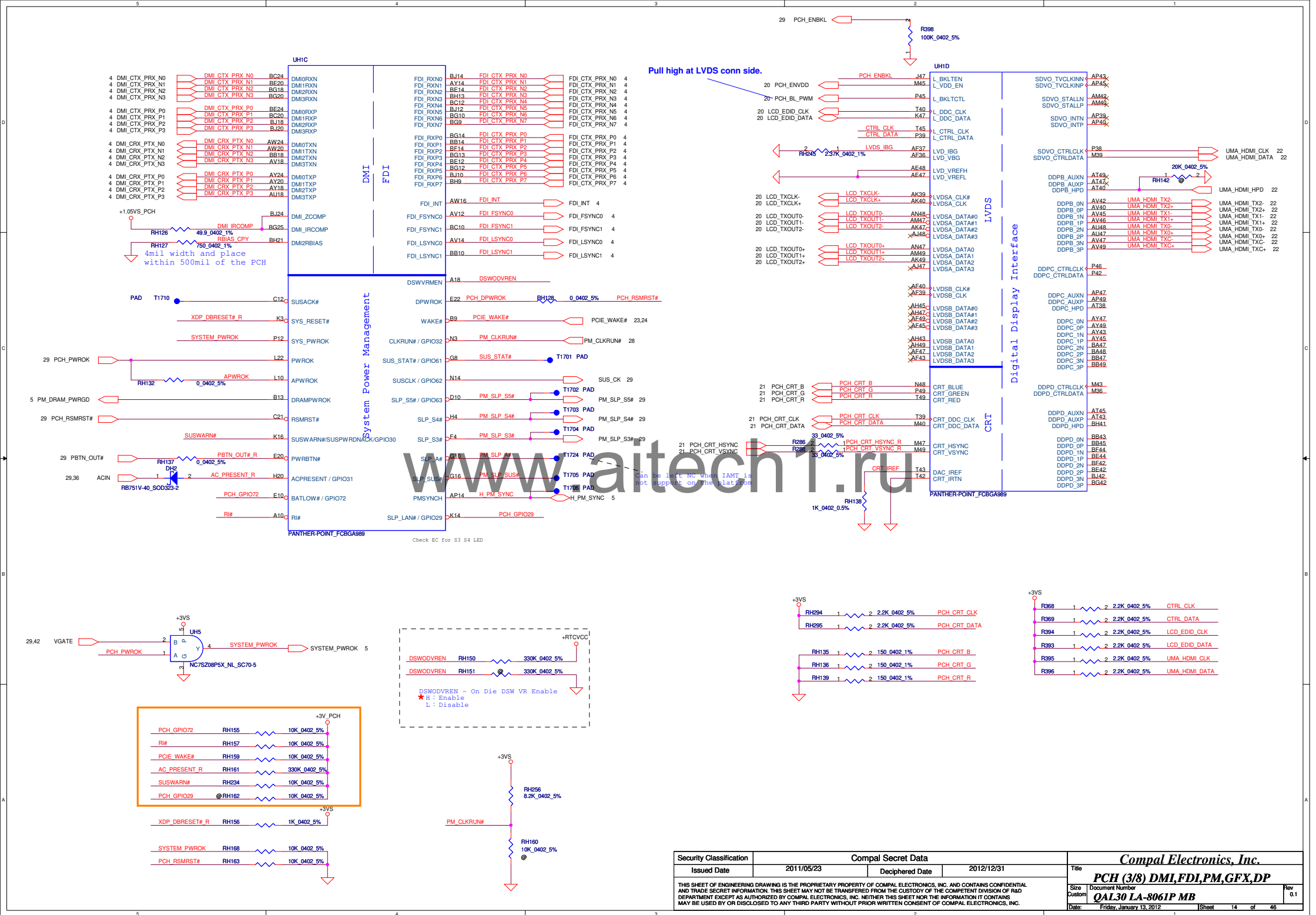
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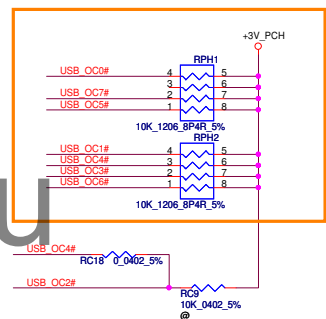
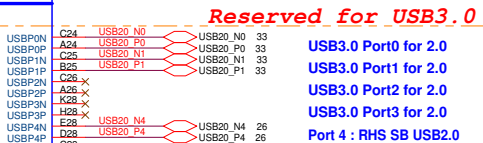
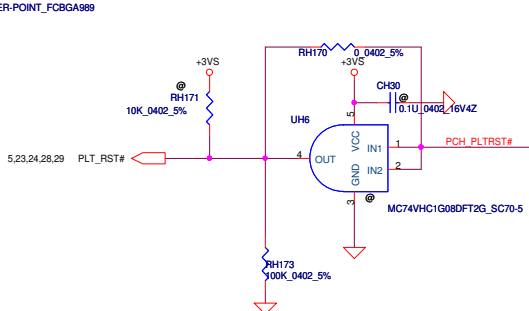
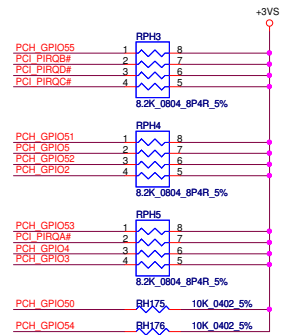
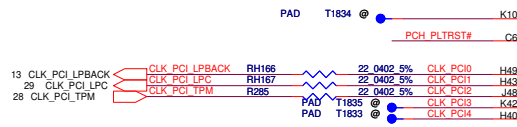
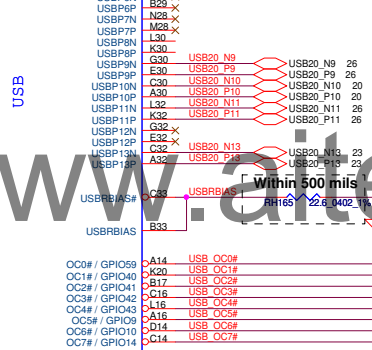
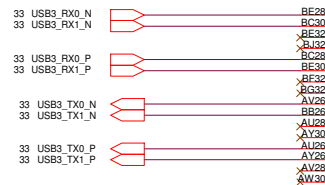






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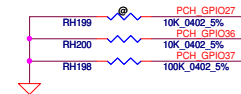
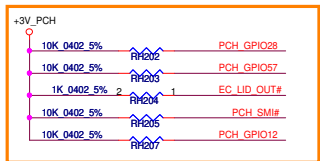
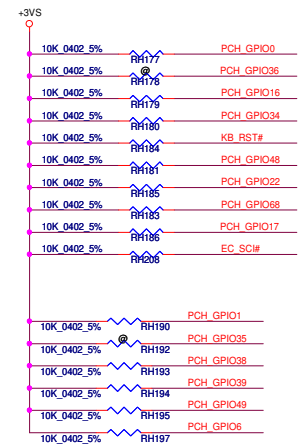




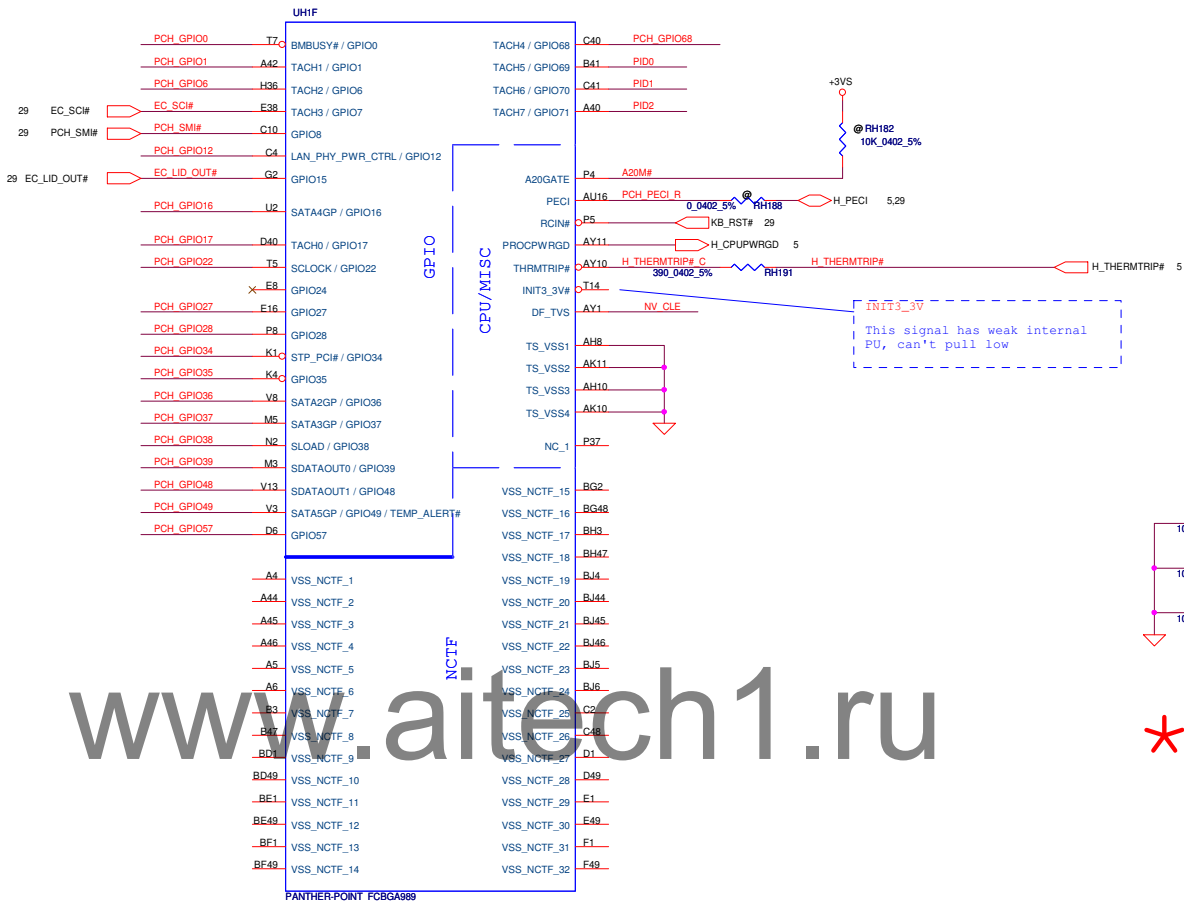
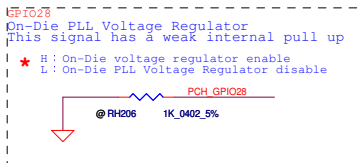
GPIO19 => BBS_BIT0
GPIO51 => BBS_BIT1

Boot BIOS Strap		
BBS_BIT0	BBS_BIT1	Boot BIOS Location
0	0	LPC
0	1	Reserved(NAND)
1	0	Reserved
1	1	SPI ★

Intel Anti-Theft Technology	
NV_ALE	High=Enabled
	Low=Disable(floating) ★



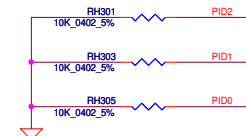
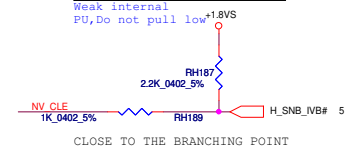
GPIO36/37
When Unused as GPIO or SATA*GP -
Use 8.2K-10K pull-down to ground.



PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

Please refer to Huron River Debug Board DG 1.2

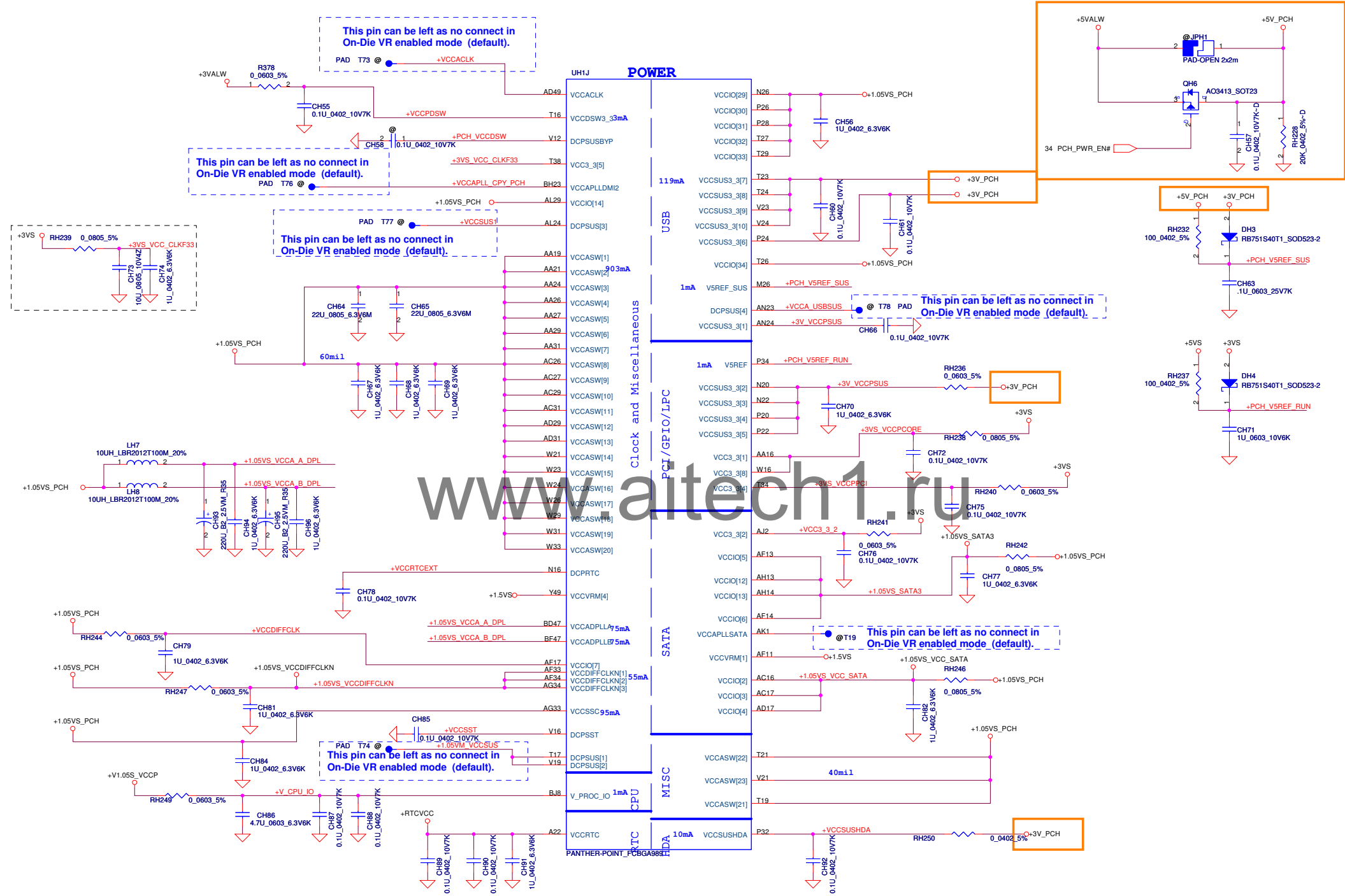
DMI Termination Voltage		
NV_CLE	Set to Vcc when HIGH	
	Set to Vss when LOW	



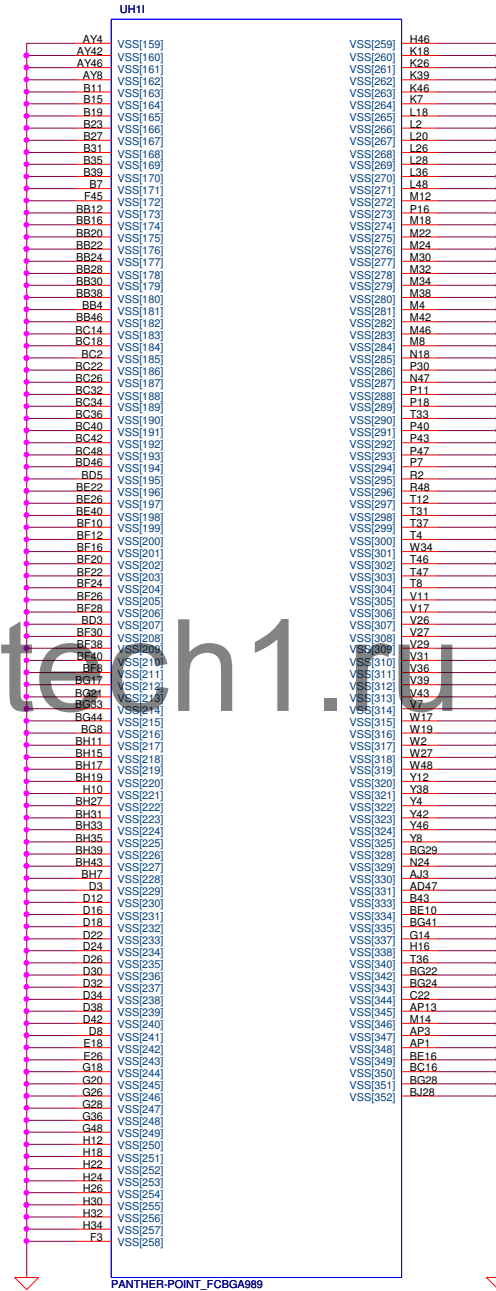
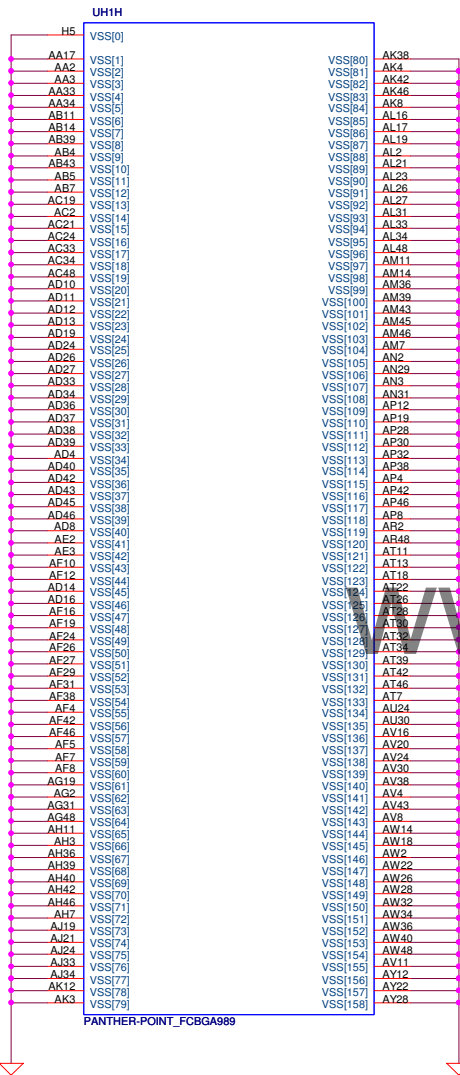
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PID :	210	
QAL30	000	(UMA)
QAL31	001	(DIS)
QAL50	010	(UMA)
QAL51	011	(DIS)
KSPD		
Q0000	1XX	

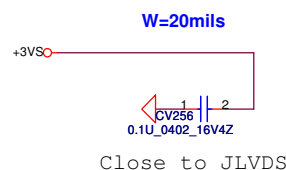
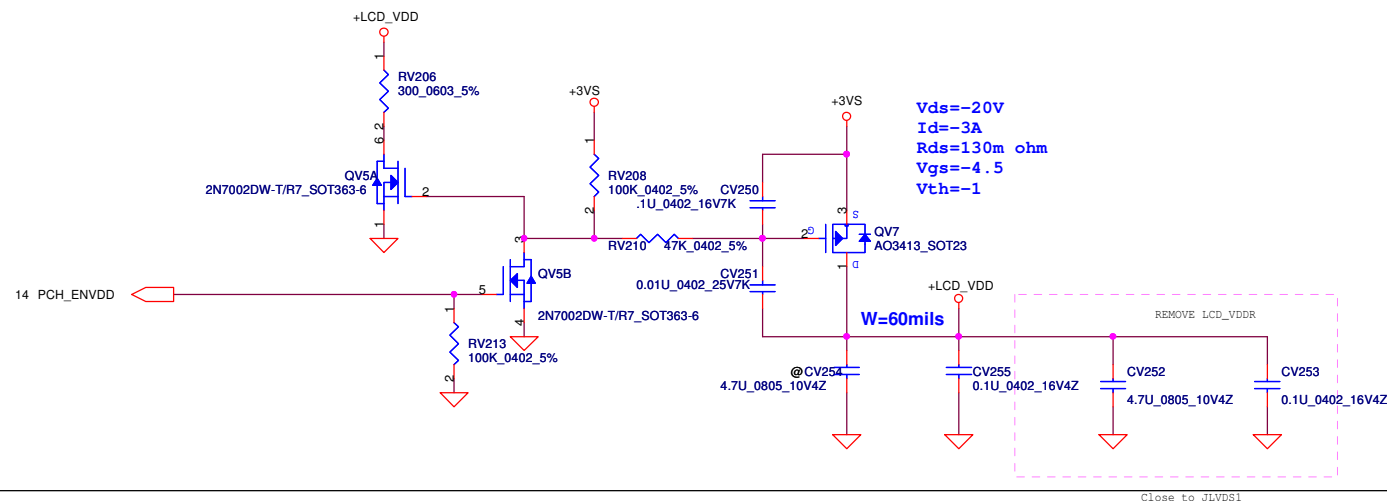
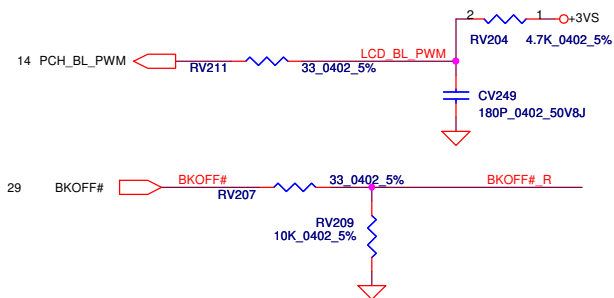
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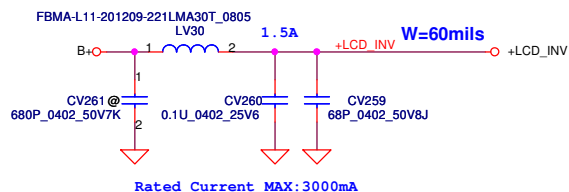
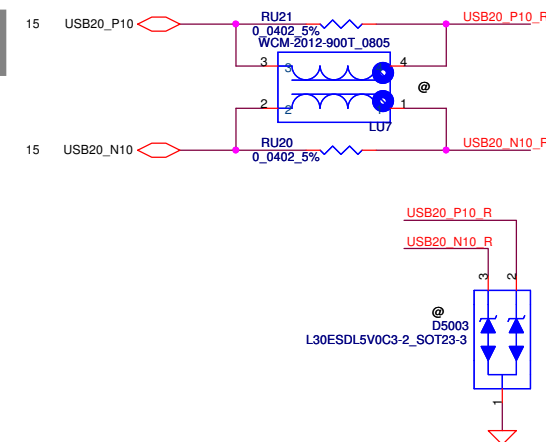
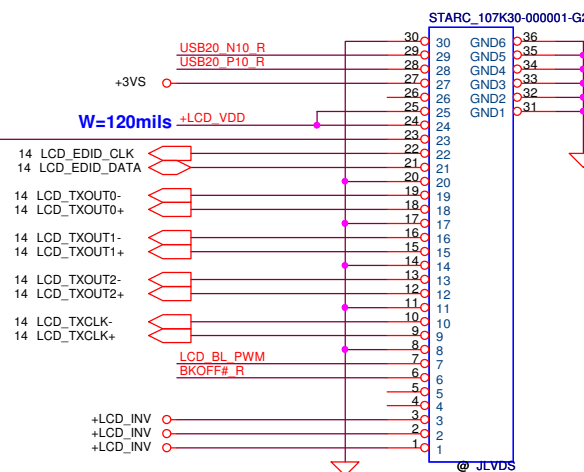
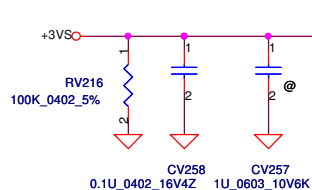
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Change to 30 pin.

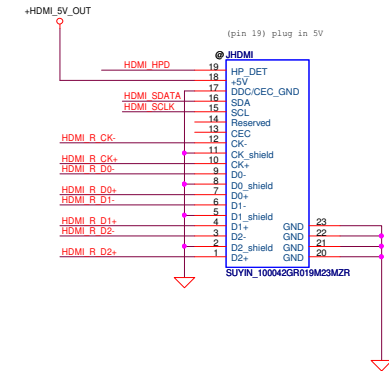
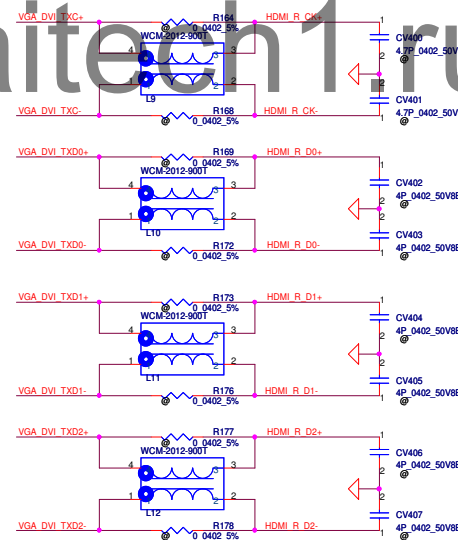
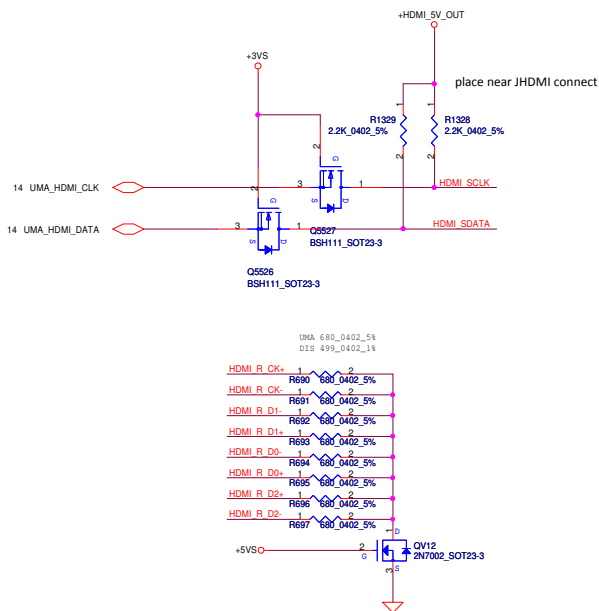
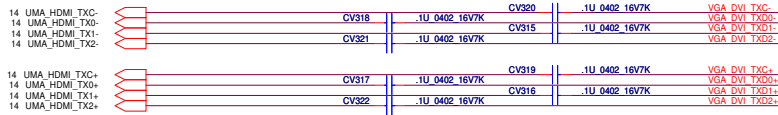
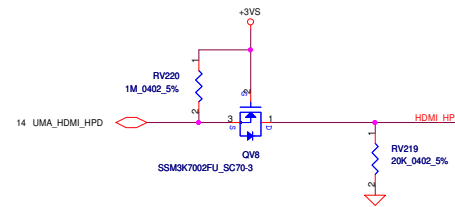
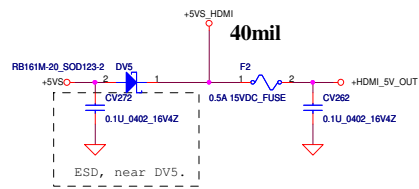
Single Channel LVDS

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LCD/PANEL BD. Conn.

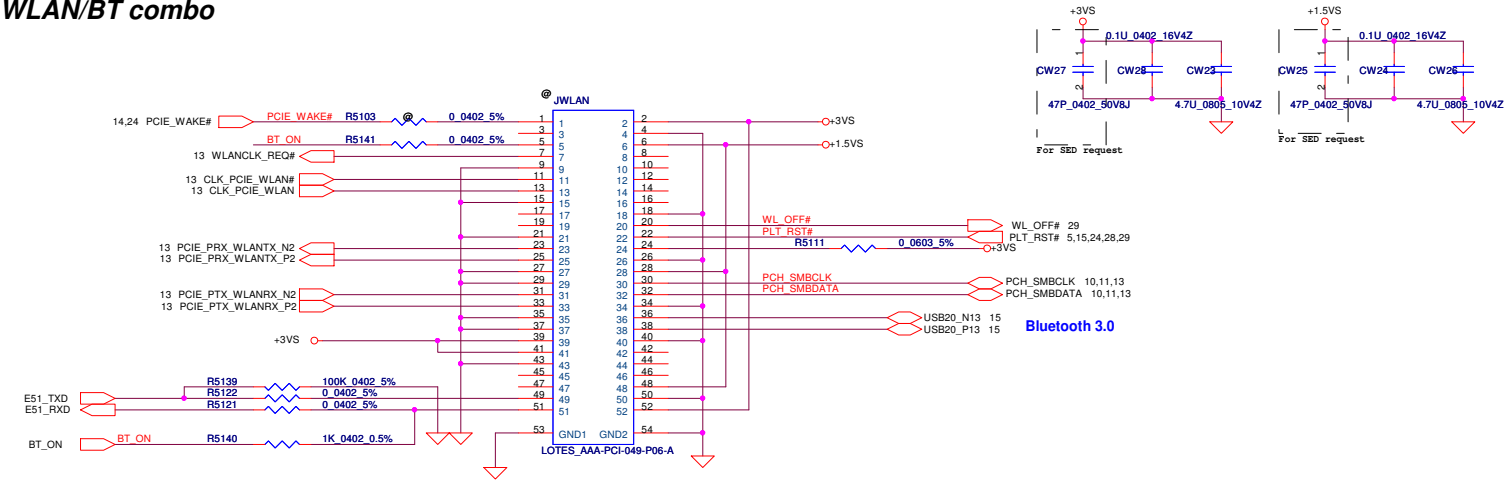
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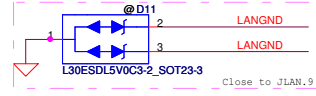
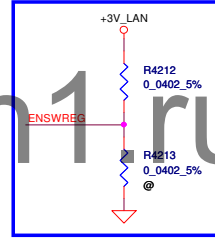
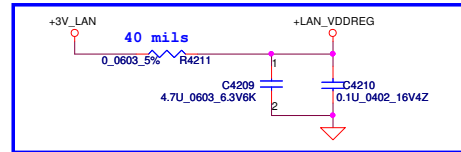
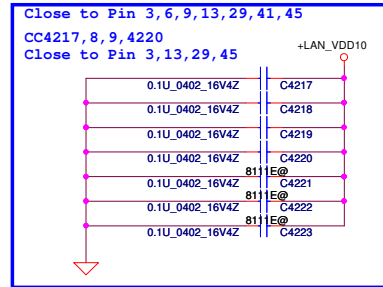
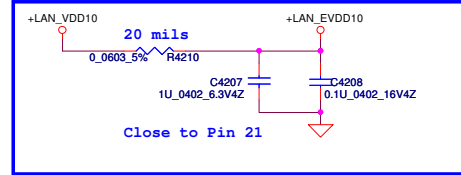
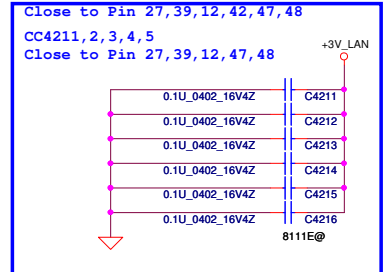
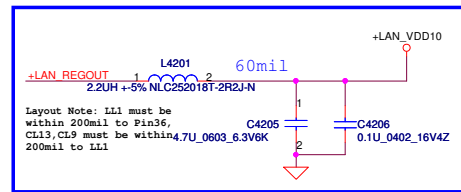
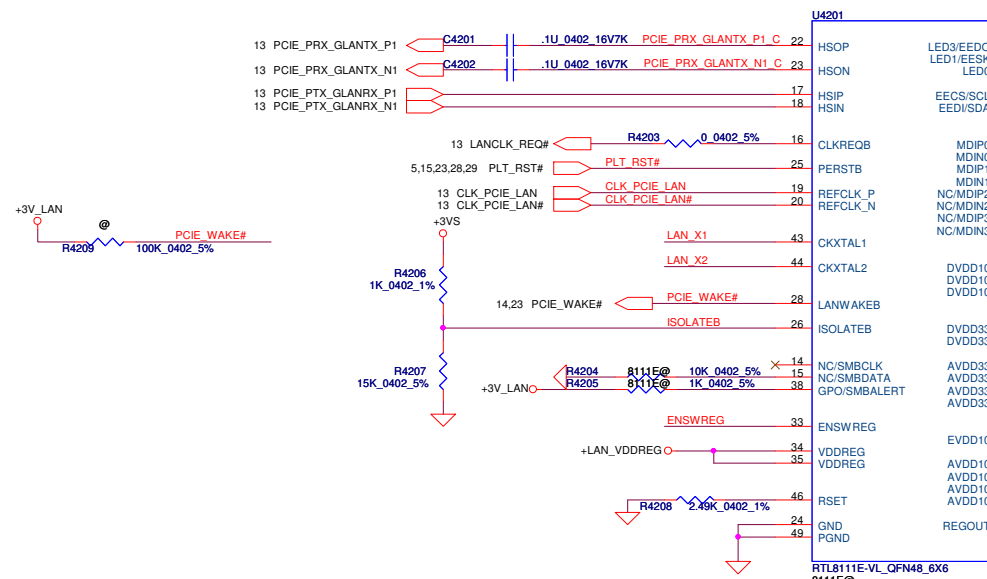
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Issued Date	2011/05/23	Deciphered Date	2012/12/31	Title
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				Size
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				Friday, January 13, 2012
				Sheet 22 of 46

WLAN/BT combo



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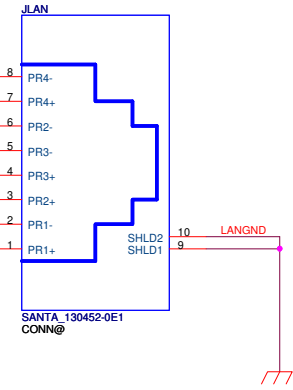
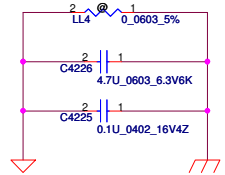
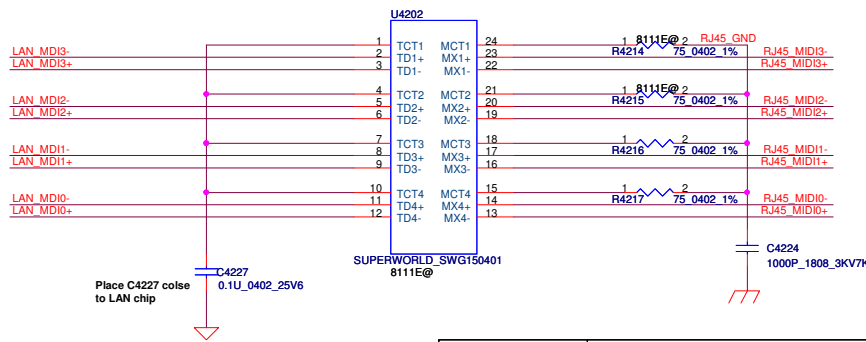
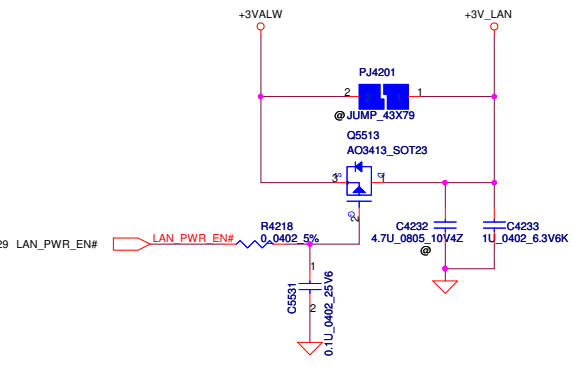
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Issued Date	2011/05/23	Deciphered Date	2012/12/31	Title	WLAN
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				Date: Friday, January 13, 2012	Sheet 23 of 46



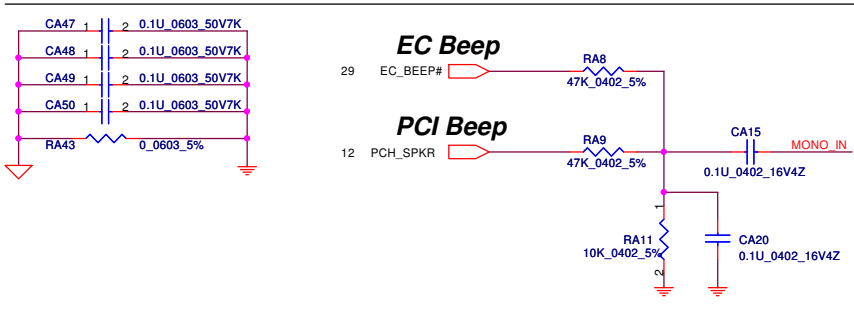
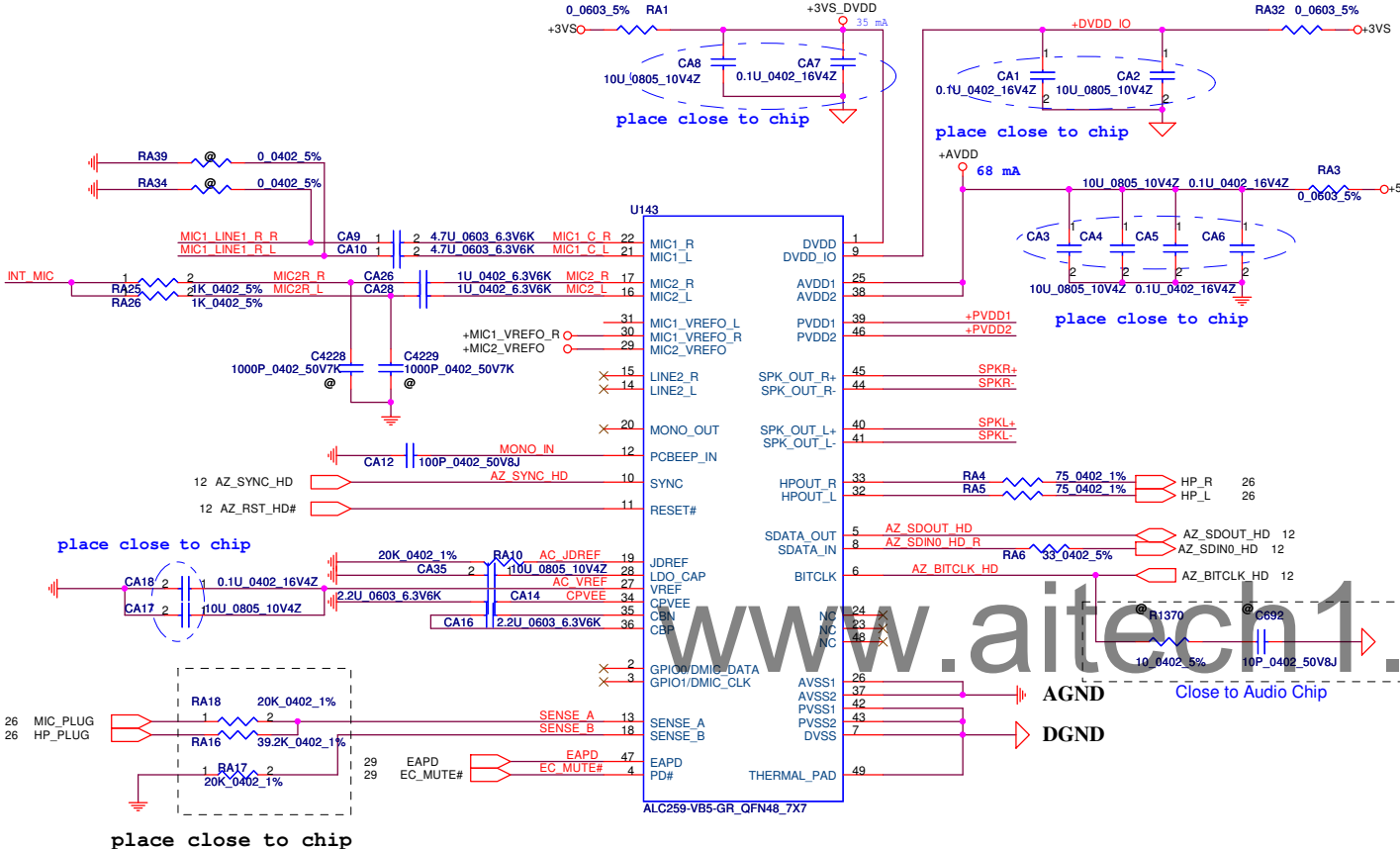
LAN Conn.

+3V_Lan Rise time(10%-90%)要>1ms and <100ms

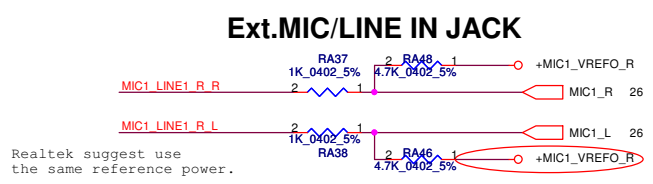
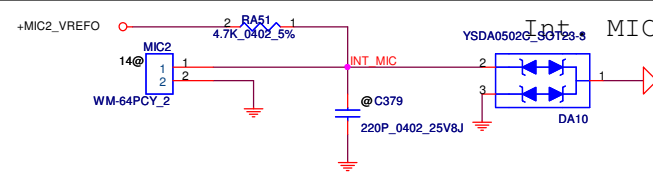
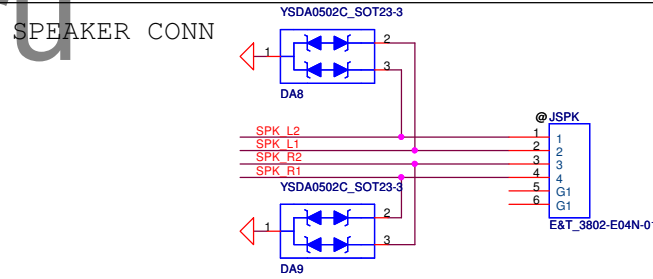
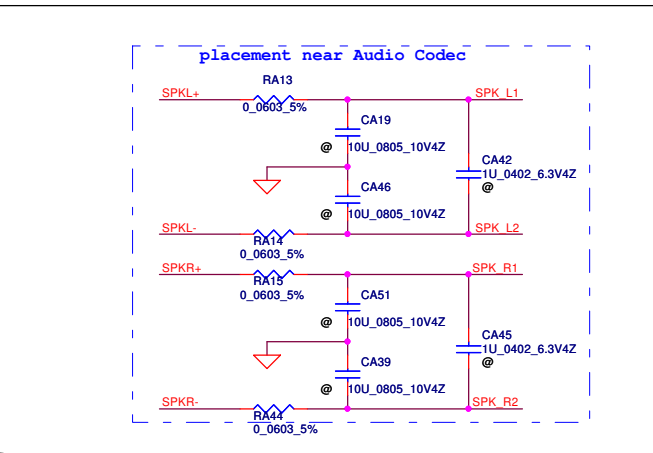
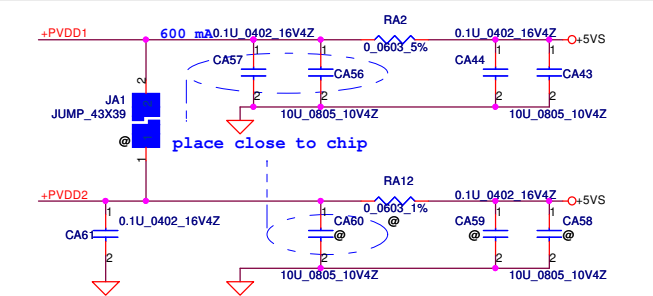
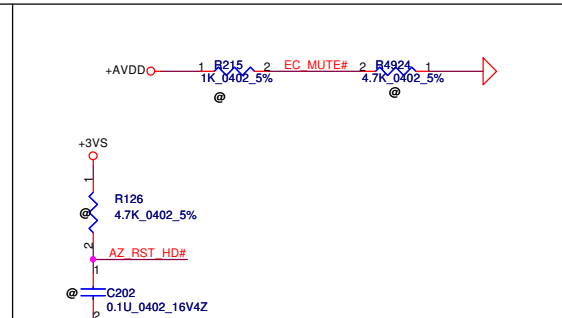
+3VALW TO +3V_LAN



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				Custom	0.1
				QAL30 LA-8061P MB	
				Date:	Friday, January 13, 2012
				Sheet	24 of 46

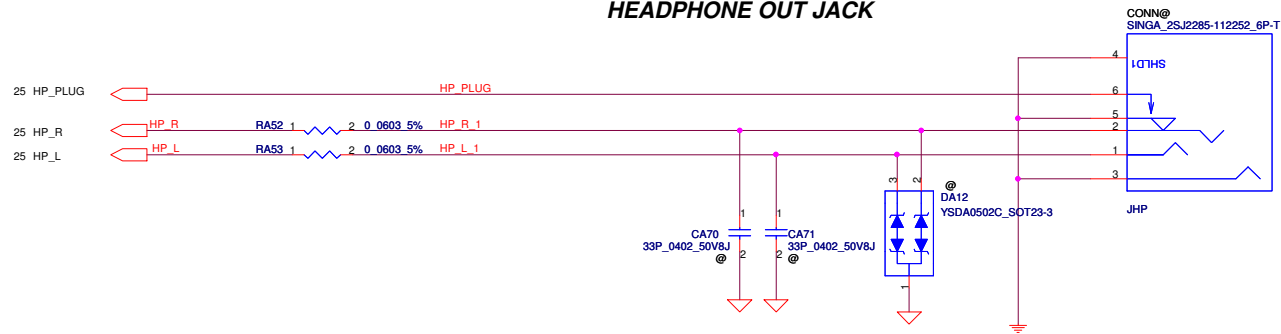


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
SENSE B	20K	PORT-F (PIN 16, 17)	Int. MIC

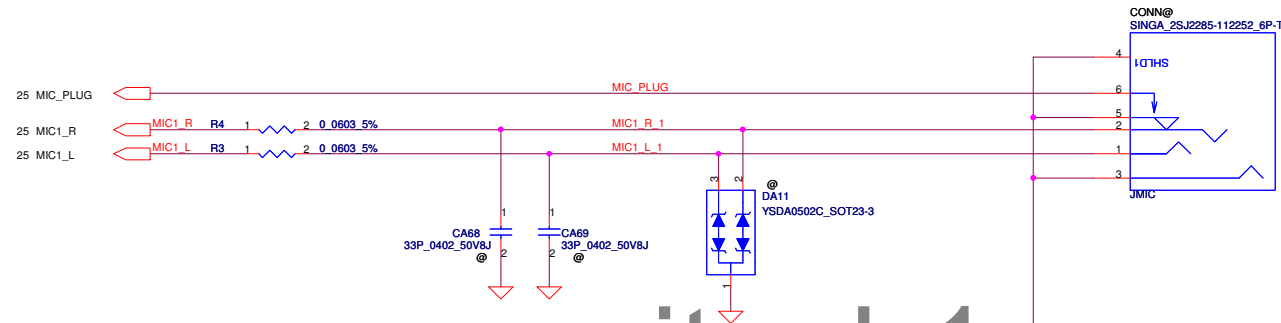


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				Date	Friday, January 13, 2012
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HEADPHONE OUT JACK

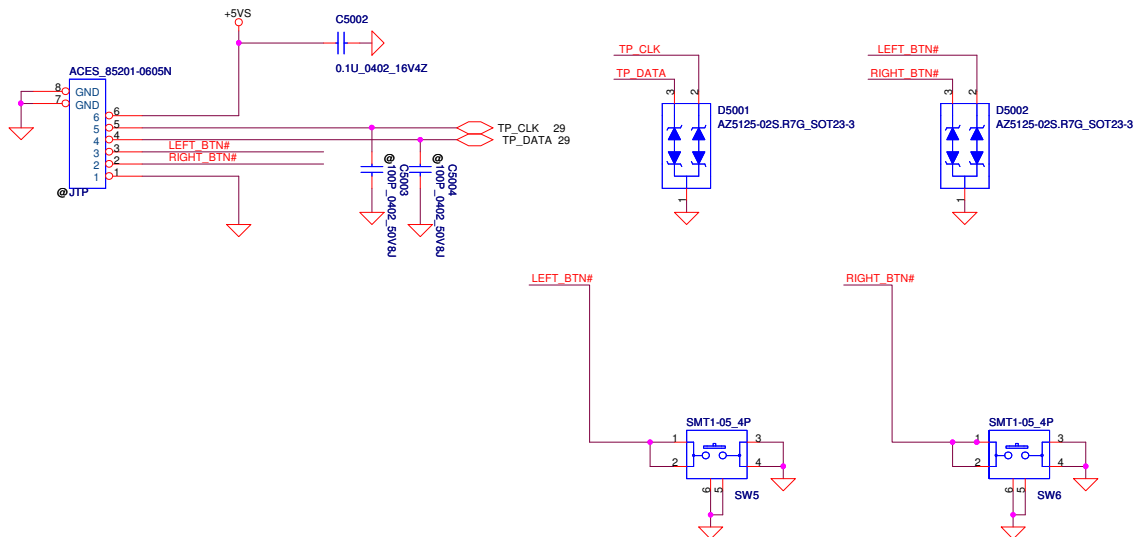


MICROPHONE IN JACK

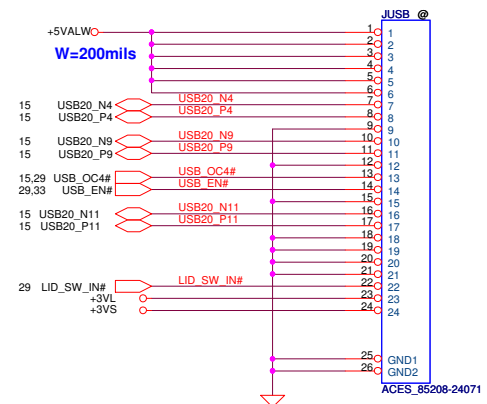


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Touch/B Connector

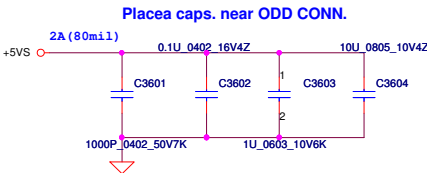
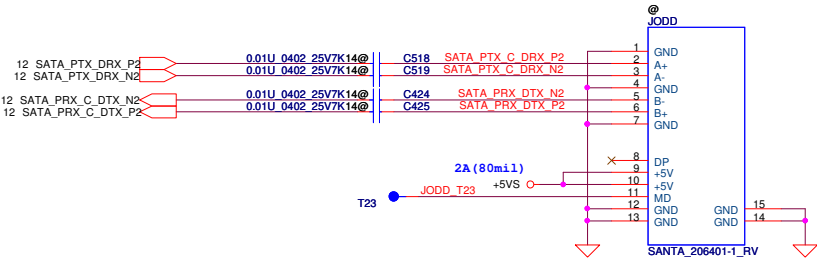


USB + LID SB



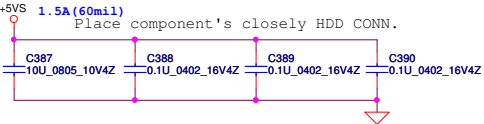
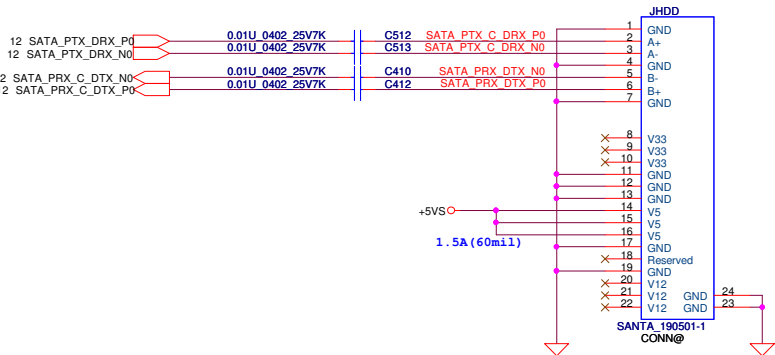
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AUDIO CONN/TP/FUNB			
Size	Document Number	QAL30 LA-8061P MB	
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SATA ODD Conn.



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SATA HDD Conn.



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				Custom	QAL30 LA-8061P MB	0.1
				Date:	Friday, January 13, 2012	Sheet 27 of 46

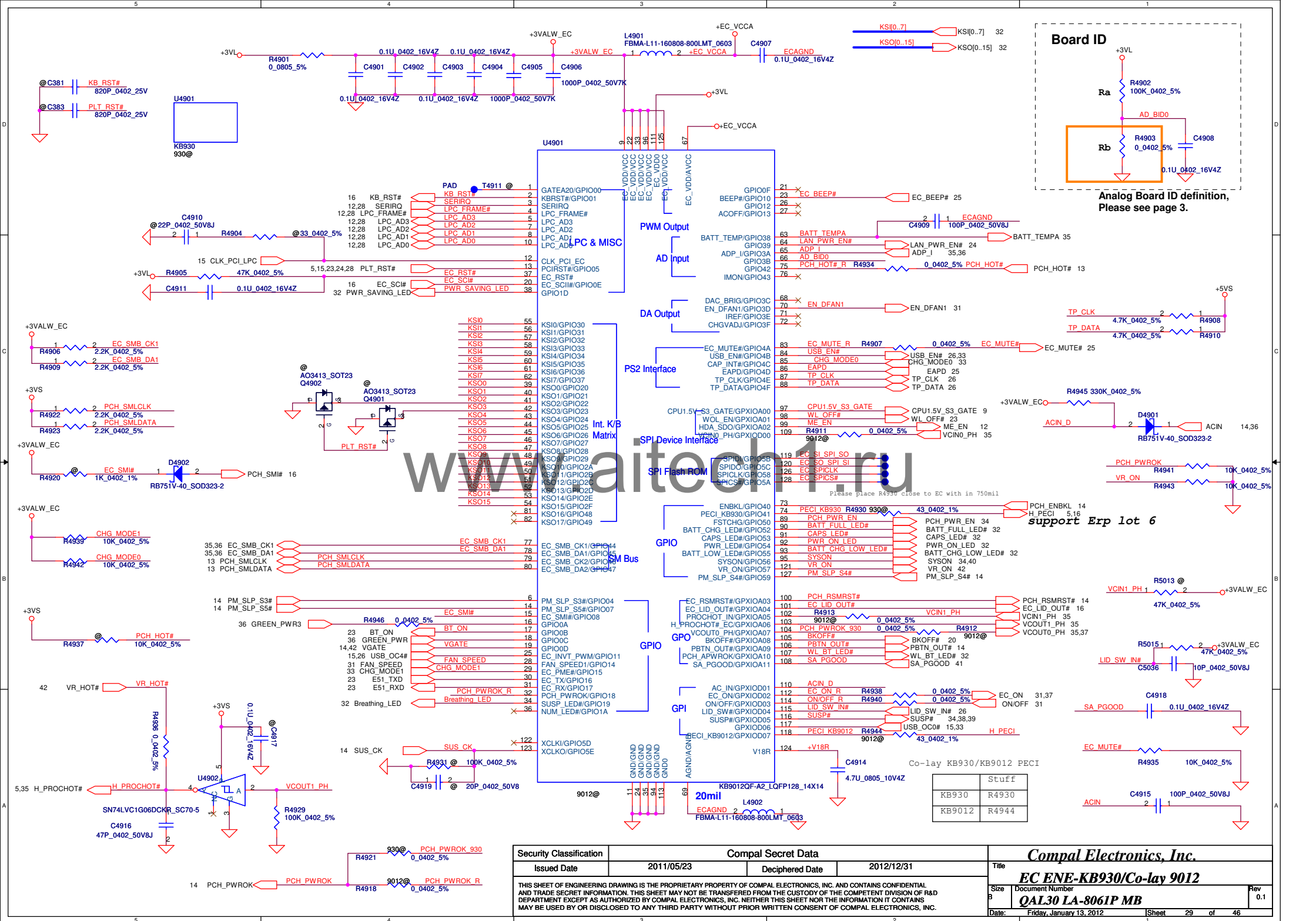
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Base I/O Address

0	=	02Eh
★ 1	=	04Eh

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				TPM	
				Size	Document Number
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				Sheet	28 of 46



BIOS Bus switch

R401

0.0402_5%

NOW8@

R402

0.0402_5%

NOW8@

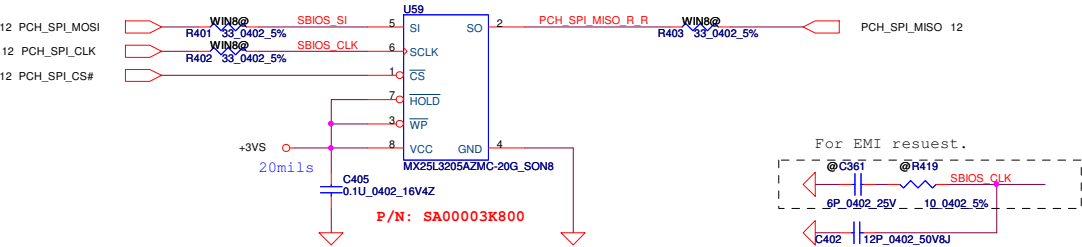
R403

0.0402_5%

NOW8@

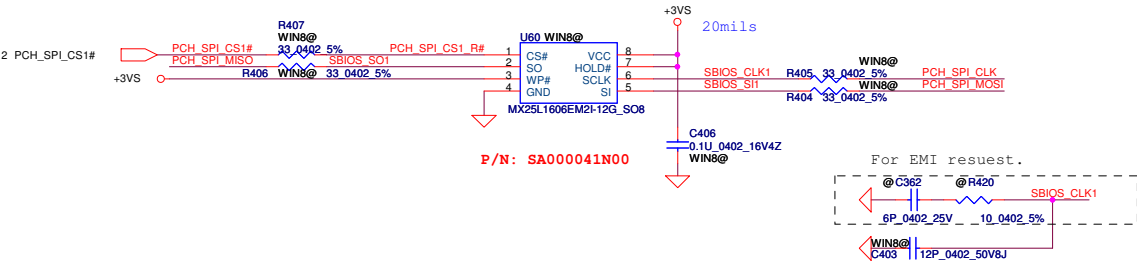
When use single ROM, use 0 ohm.

BIOS SPI Flash (4MByte*1)



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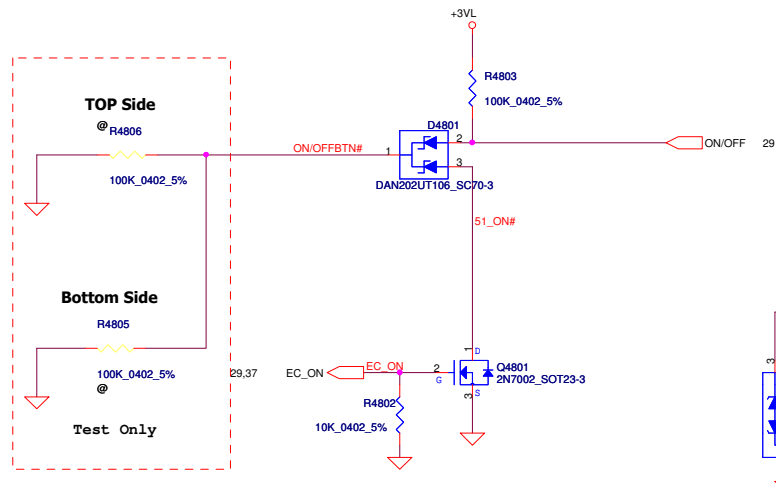
BIOS SPI Flash (2MByte*1) For Win8



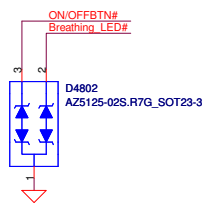
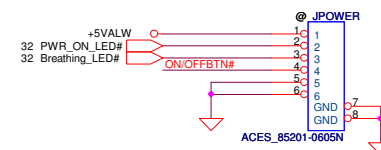
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Issued Date	2011/05/23	Deciphered Date	2012/12/31	Title	
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				Size	Document Number
				QAL30 LA-8061P MB	
				Date:	Rev
				Friday, January 13, 2012	0.1
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				30	46

Power Button

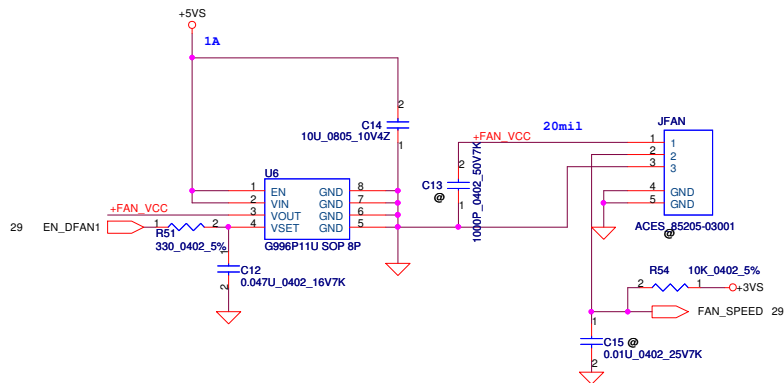
ON/OFF switch



To POWER/B

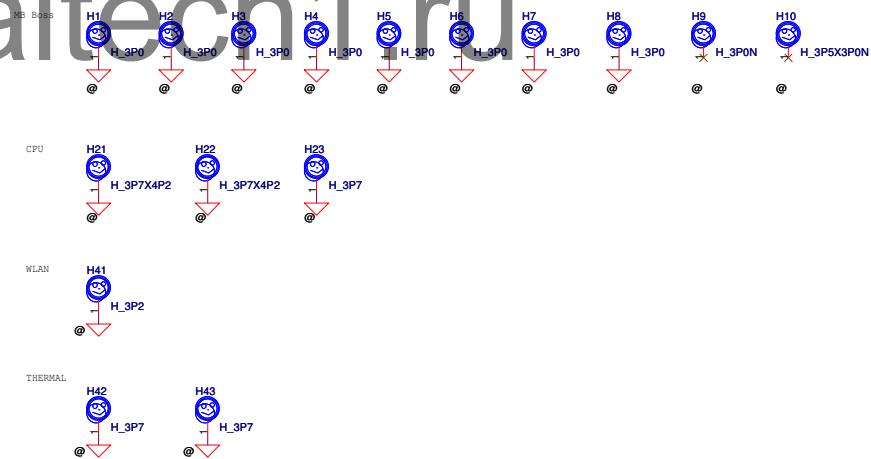


Fan Control Circuit



Screw Hole

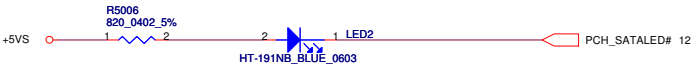
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LED

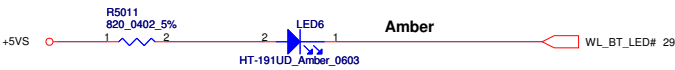
SATA



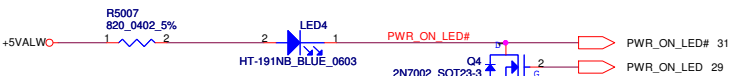
Battery



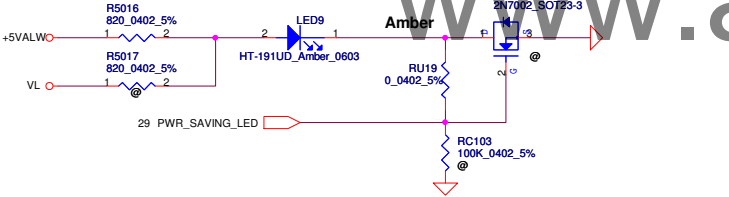
Wireless



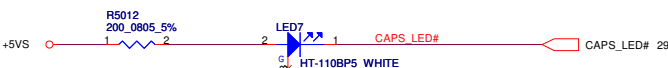
Power



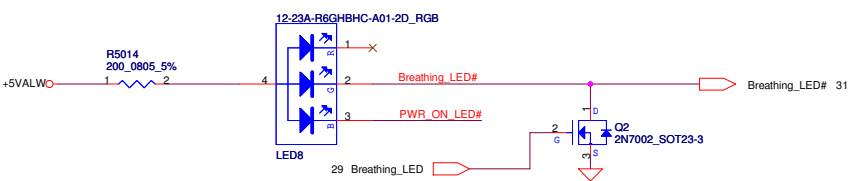
Power Saving



CAP Lock



Breathing



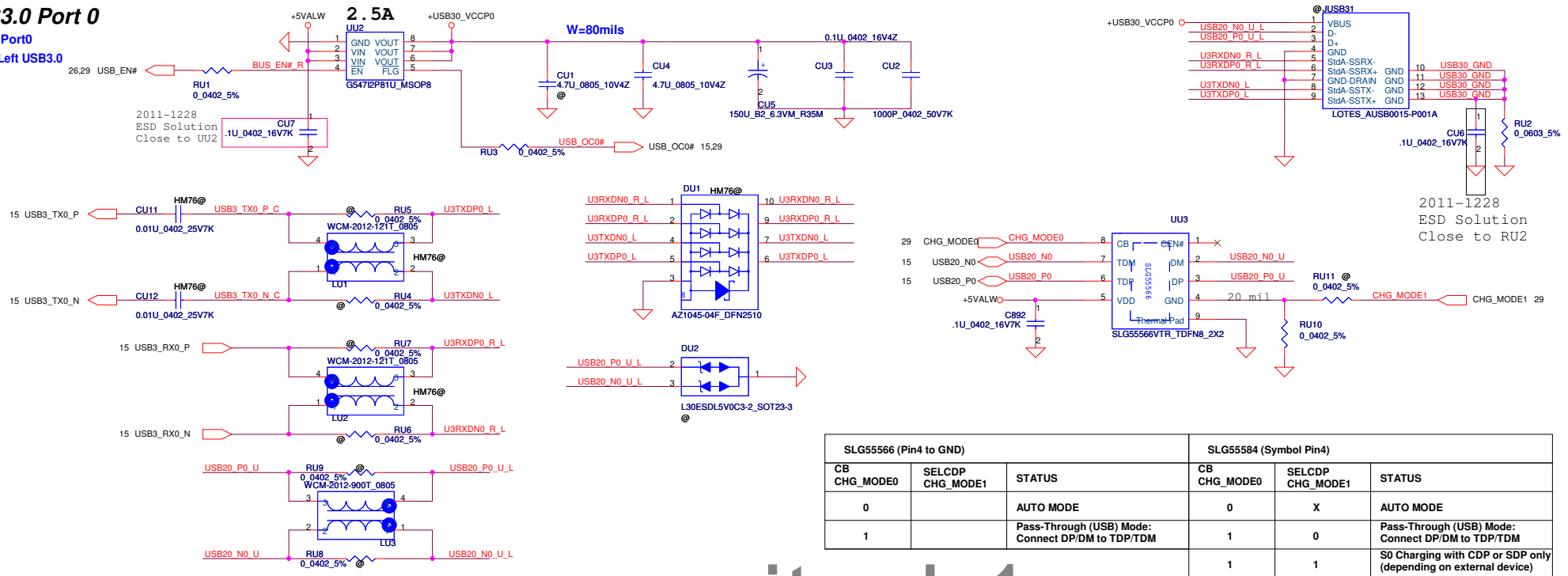
INT_KBD Conn.



USB3.0 Port 0

USB3.0 Port0

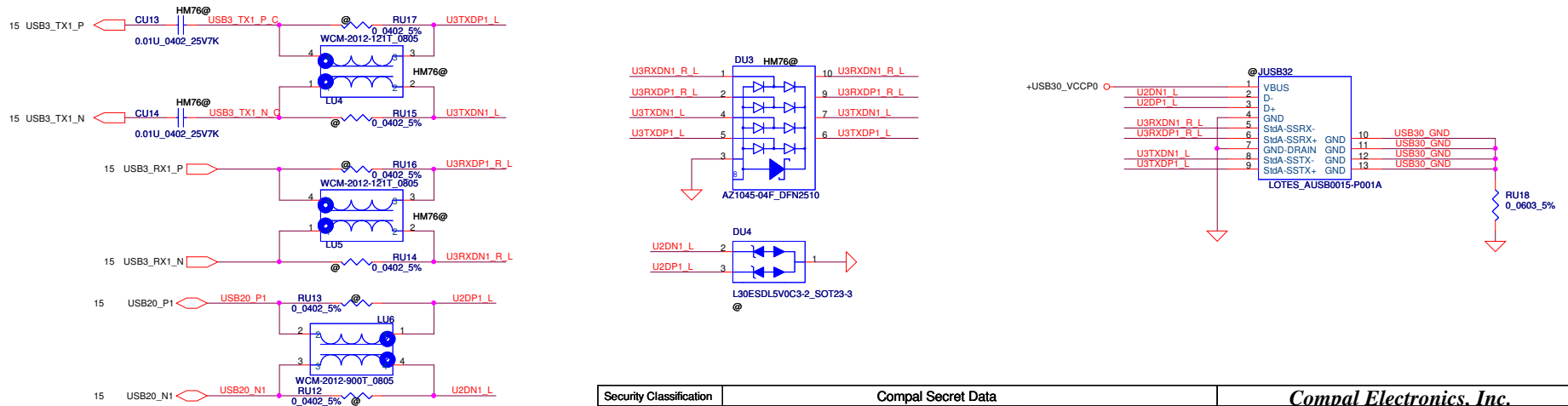
Port 0 : Left USB3.0



USB3.0 Port 1

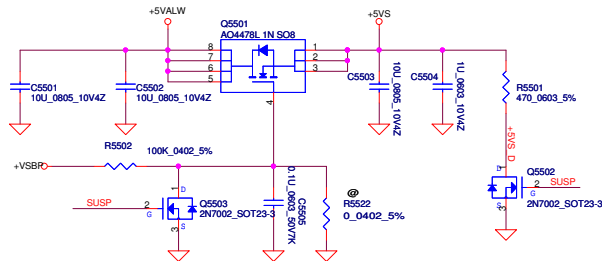
USB3.0 Port1

Port 1 : Left USB3.0

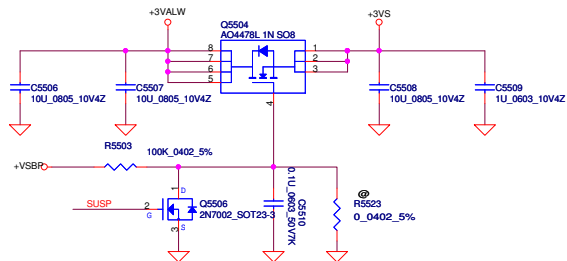


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Issued Date				2011/05/23				Title			
				Deciphered Date				Power share ENE3810			
				2012/12/31				Size			
								Customer			
								QAL30 LA-8061P MB			
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								Friday, January 13, 2012			
								Sheet			
								33 of 46			
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								0.1			

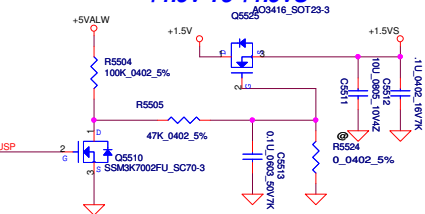
+5VALW to +5VS



+3VALW to +3VS

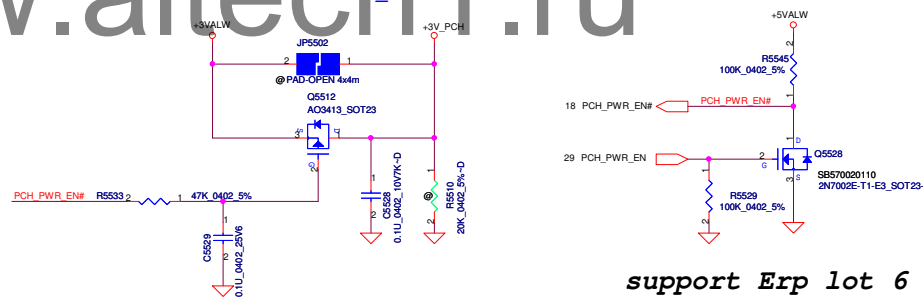


+1.5V To +1.5VS



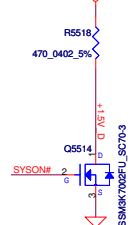
CHECK WITH CPU memory power

+3VALW to +3V_PCH

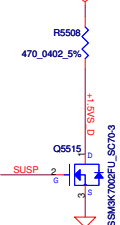


support Exp lot 6

+1.5V



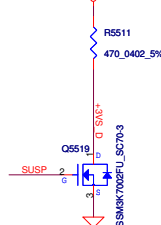
+1.5VS



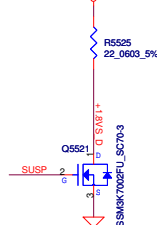
+V1.05S_VCCP



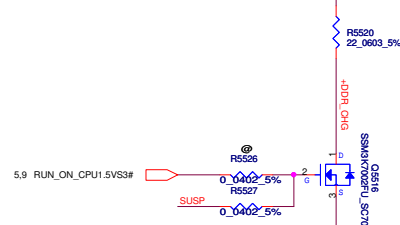
+3VS



+1.8VS

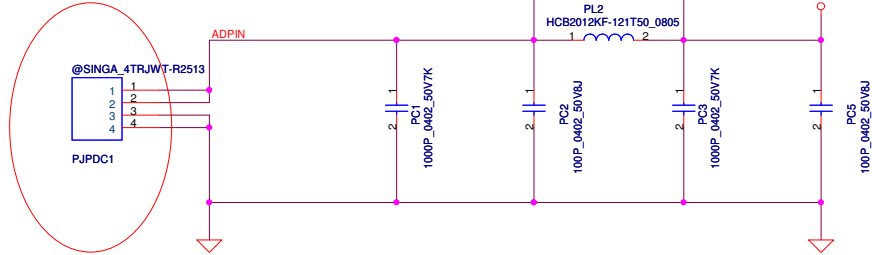


+0.75VS



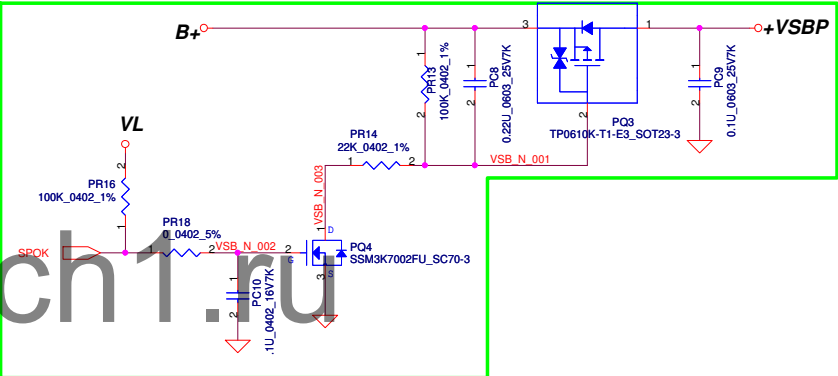
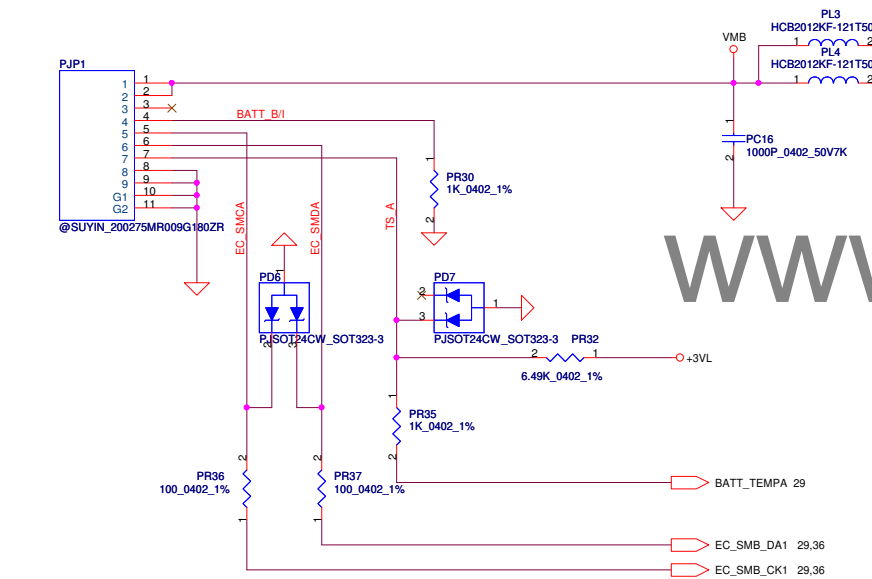
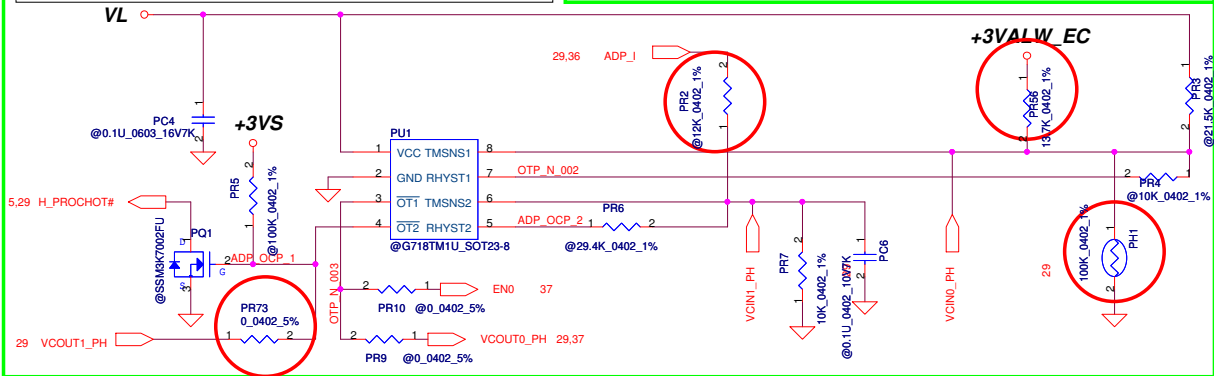
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				Size
				Custom
				QAL30 LA-8061P MB
				Rev
				0.1
				Date
				Friday, January 13, 2012
				Sheet
				34
				of
				46

DCIN jack P/N:DC301008L00,
need dogle confirm P/N with ME



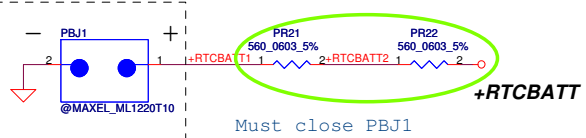
PH1 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU1 circuit, but keep PR56
PH1, PR2, PQ1, PR7,PQ15,PR73,PR56



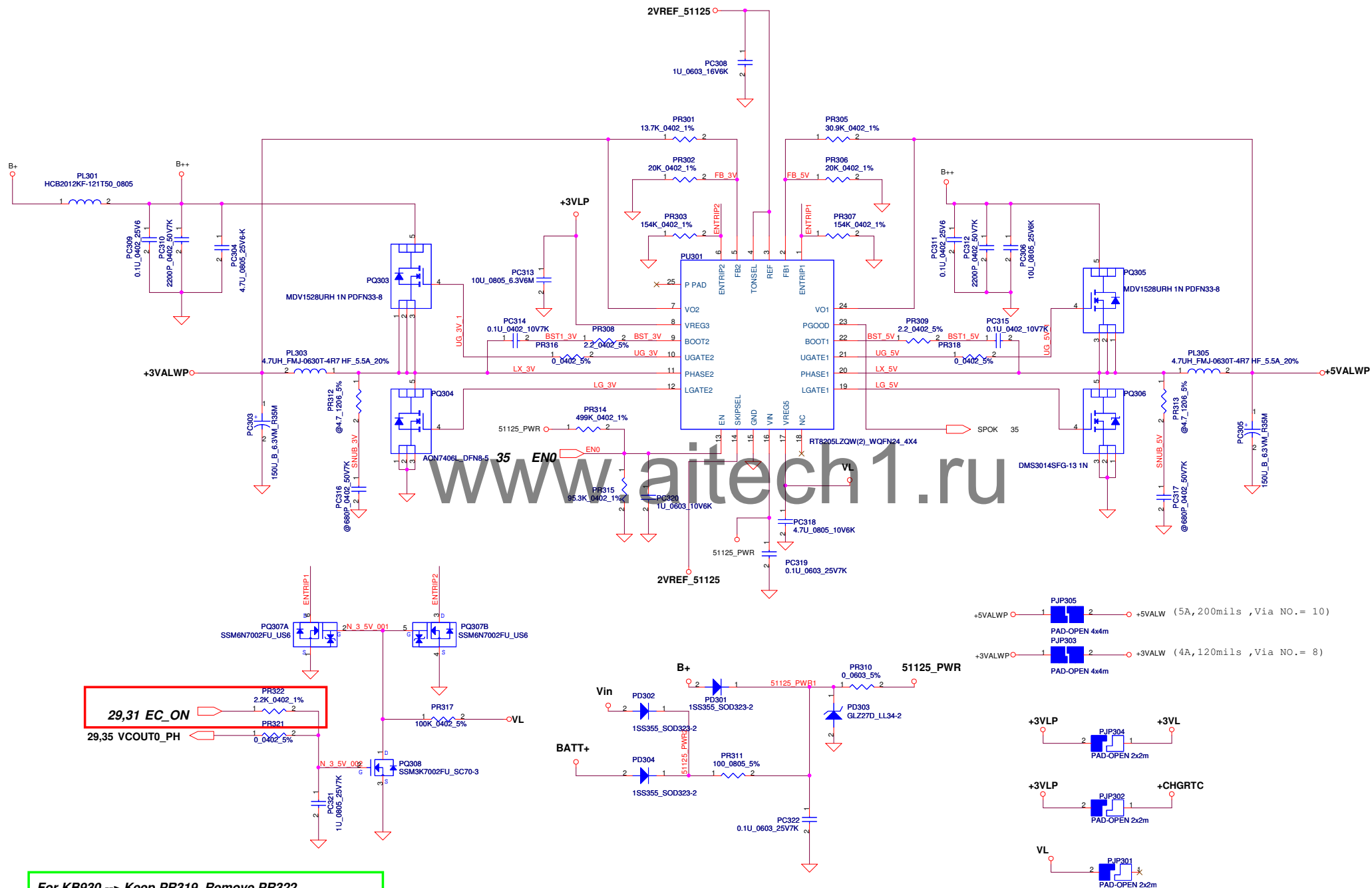
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RTC Battery



SP093MX0000
Change RTC For Cost Down

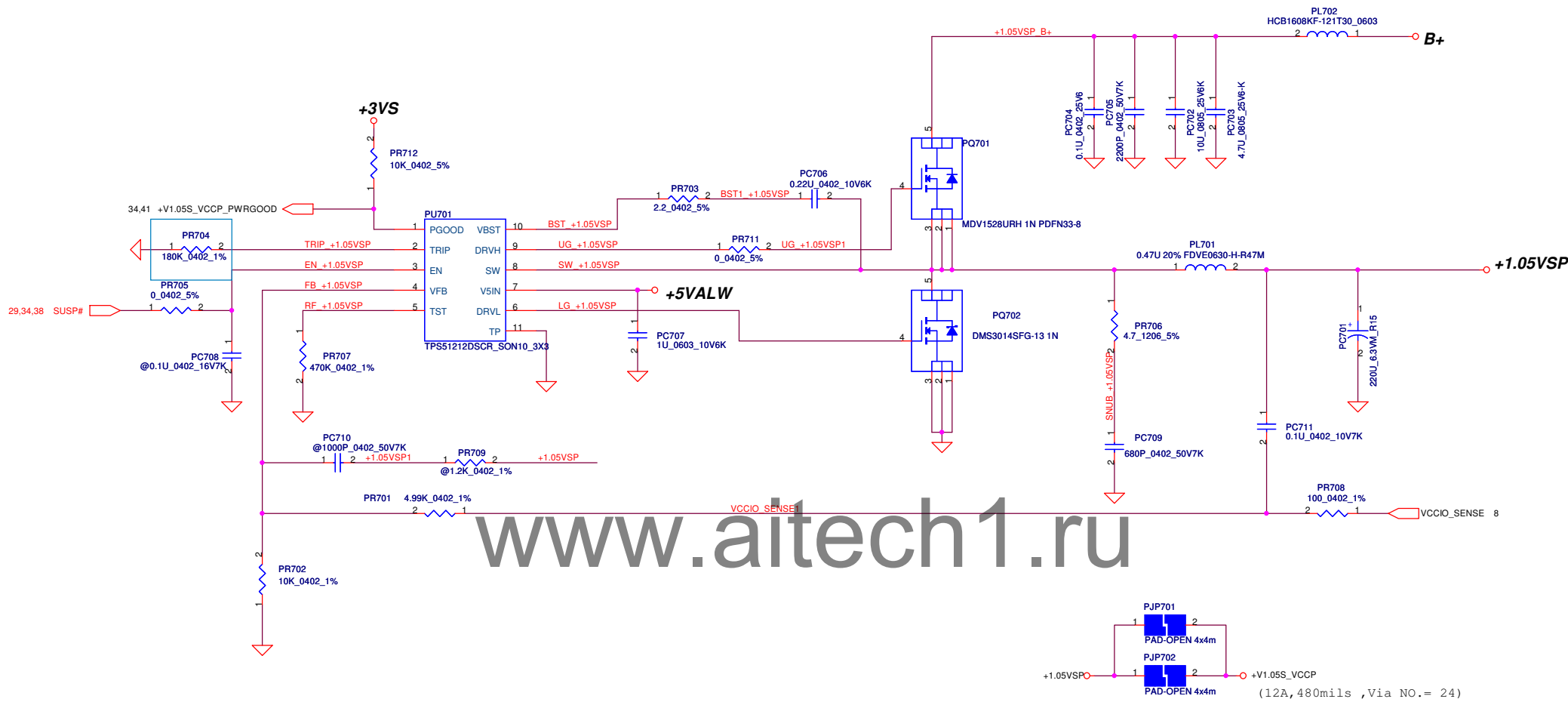
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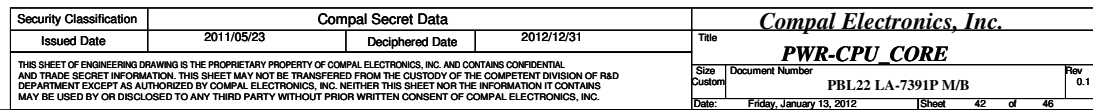


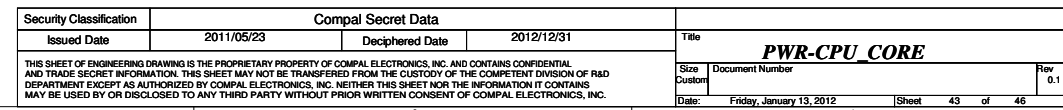
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+5VS 

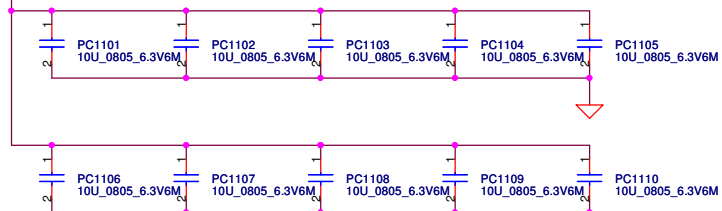
VSPA, VSNA to GND (HW side). FBA and COMPA are short.

DIS only:
All AXG components are @.
Except
PR272 and PR273 are 0ohm.
PC223, PC226, PR202 are 0ohm.
PC220, PC215, PR206 are 0ohm.

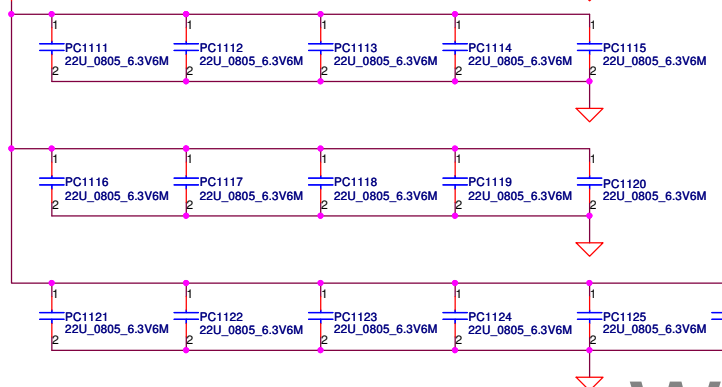




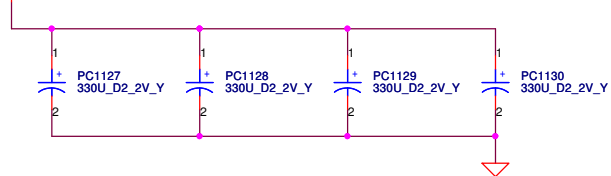
+VCC_CORE



+VCC_CORE



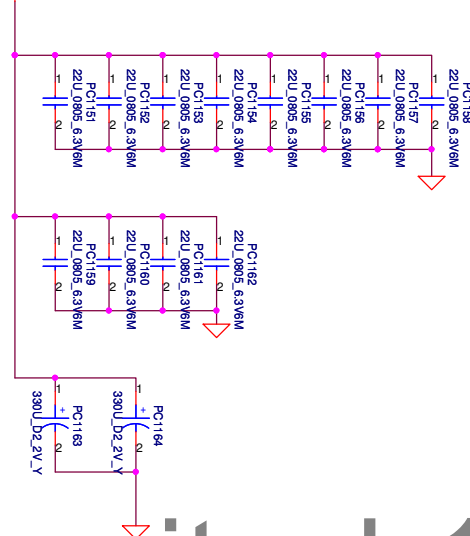
+VCC_CORE



+VCC_CORE

+GFX_CORE

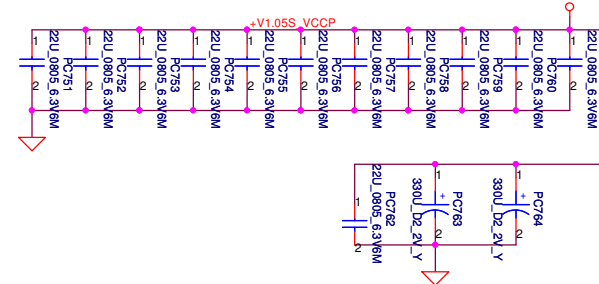
+GFX_CORE



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

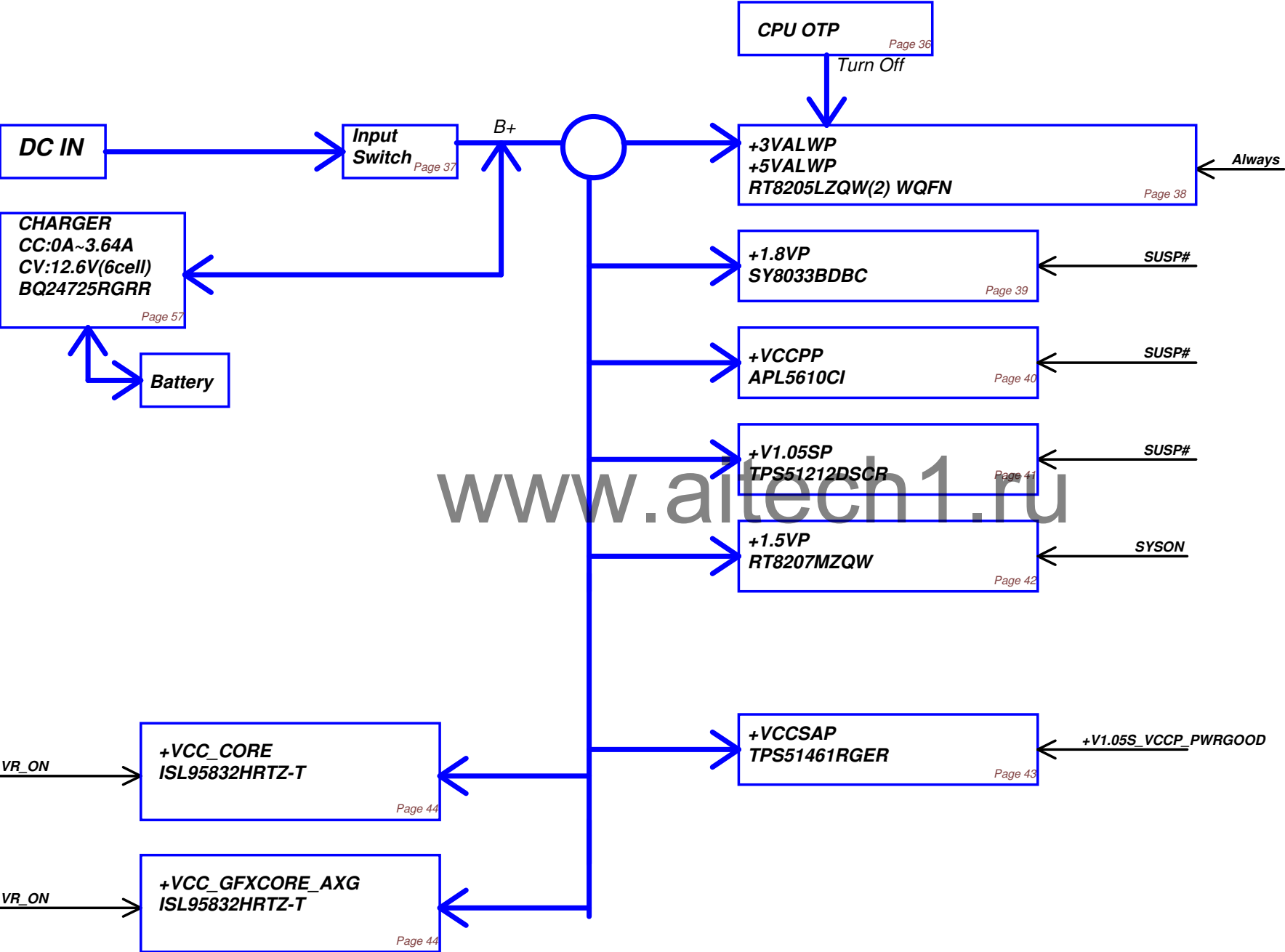
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Power block



Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1					PR504 change from 15K to 15.4K		
2					charger IC change form bq24725A to bq24735		
3					PQ104,PQ303,PQ305,PQ701 charge form SIS412DN to MDV1528URH		
4					PQ306 charge from AON7702L to FDMC7692S		

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